Design of power-efficient two-stage dynamic comparators for biomedical Signal acquisition in 90nm technology

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Abstract

Dynamic comparators are very essential for any signal processing and acquisition system which is used for the monitoring of physiological signals (Electrocorticography (ECoG) and Electro cardiogram (ECG) signals). In this paper, a novel design for dual tail dynamic comparator is proposed. The proposed design consumes only 11.4uW power. The offset-voltage of design is determined as 1.33mV, which is less than the existing design. Delay of the system is found as 260 ns, which is also comparable with existing systems. In the design, PMOS transistors in the preamplification stage is connected in a cross-coupled manner to increase the pre-amplifier stage gain. The design is carried out in 90nm CMOS technology in CADENCE Virtuoso. A clock signal of 1 GHz is being used for sampling process.

Keywords: Low power, Dynamic Comparator, Single stage dynamic comparator, Double tail dynamic comparator, bio-physiological systems, Mixed signal processing

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1. INTRODUCTION

Data converters (ADC) are an integral part in the mixed signal processing systems like biological signal acquisition or monitoring [1]. Many of these devices are battery powered and portable in nature. Sophisticated devices like cardiac pace-maker and cardiodefibrillator are also body implantable. In the case of implantable medical devices, the battery life is of utmost importance and it is proportional to the power that is being drawn from the battery. To make an ADC power efficient, the various building blocks inside it must consume less power. Comparator plays a vital role in the data converter circuit[2, 3, 4].The main purpose of comparator is to compare two input signals and produce an output according to the incoming signals. Reduction of comparator power the power reduces the total power dissipated in the ADC. Various research methodologies have been proposed in previously published literatures to make the comparator power efficient [5, 6, 7, 8]. Along with power, accuracy and speed of operation of comparator are also important. Initially, static comparators were being used

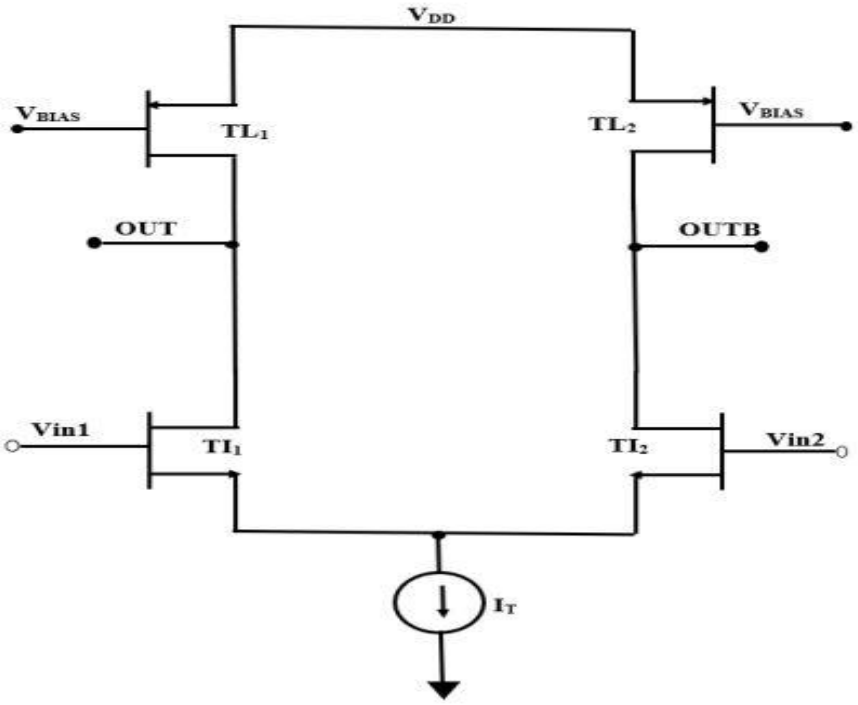

Fig.1 Static Comparator circuit with active load

(Fig.1). But these could not satisfy the low power and speed requirements. As a solution, dynamic comparators were introduced. A general comparator block diagram is given in Fig.2.

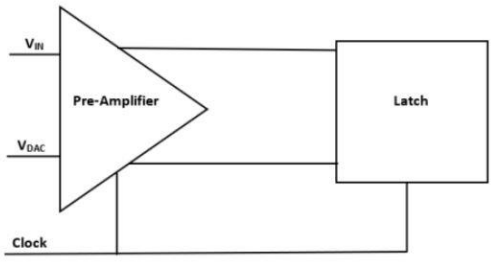

Fig.2 General Comparator Block

Single stage dynamic comparators are prone to kick back noise which introduces non linearity errors [9, 10]. New age dynamic comparators have two stages of operation [11]. First is the pre-amplification stage, which receives the input signals to be compared. The second one is a regenerative latching stage which gives desired output. The positive feedback provided in the latching stage improves the comparison speed. These two-stage comparators are often referred to as double tail comparators. One tail transistor is used in the pre amplification stage and the second one is used with latching stage.

Dynamic comparator presented in paper [12] has higher operating speed. However, the design suffers from larger power consumption. Two-stage dynamic comparator presented in [13] offers lower offset voltage with a new offset cancellation technique. Although this technique is capable of reducing the transistor size and power, it increases the delay. Since biophysiological signals are having very low frequency components, it can be effectively used for conversion of low frequency signals. The design proposed in [6] is good for high-speed applications, but it consumes more power. The work reported in [14], is suitable for high-speed comparison purpose. The power reported in this work is not apt for ultra-low power applications. A low offset two stage comparator which consumes less power is discussed in [7], which offers less mismatch in the latch regenerative stage. Moreover, the transistors in the pre amplification stage are made large to minimize the offset effect. However, this increases the dissipation of power. The work reported in [15] is a fast comparator with less kick back noise. In fact, the power consumption of this comparator is regarded as high when it comes to the design for implantable biomedical devices.

A charge sharing reset method is proposed for comparator in [16]. The speed of the design as well as its power prospect is enhanced by this design. However, this design does not prevent the kick back effectively. A low supply volage (0.3V), design is given in [17]. Here forward body biased method is used for the pre-amplification and the regenerative latching stage, which effectively increase the operation speed of the circuit. In terms of conversion accuracy, more works can be done on the said design, since this design is having higher offset voltage.

To overcome the high offset voltage in comparators, an alternate design is proposed in [6]. The design reduces the pre-amplification power consumption by stopping the preamplifier, once the output has been determined by the latch stage. Additional control circuit is needed to implement this functionality. The downside of this design is the increased area and complexity of the circuit. IC's for implantable medical devices are to be area efficient.

In this work, a two-stage, less power and less offset comparator is proposed. The complexity of this circuit is reduced by using less transistor count in the circuit. The offset of the proposed design is also less compared to many recently published works. The remaining sections are

arranged as follows. In the second section conventional dynamic comparators are discussed. In Section 3, the proposed design for dynamic comparators is analysed. The result and discussion is in Section 4. The conclusions derived are given in Section 5.

2.CONVENTIONAL-DYNAMIC COMPARATORS

2.1 Conventional one-stage Single Tail Dynamic comparator

Basic circuit of a one-stage single tail comparator is given (Fig 3). This works in two phases. When the clock is low (CLK =0), the circuit enters in to pre-charge state. Under this condition the pre-amplifier tail transistor (Tt1) is OFF. Two outputs (OUT and OUTB) are charged up to supply voltage (VDD) via transistors T7, T8 (Low clock signal turns on the transistor T7 and T8, since they are PMOSFETs). The high node voltages keep the transistor T3 and T4 ON.

By enabling the clock (CLK = 1), the circuit starts the evaluation phase process. The transistor Tt1 is ON and T7 and T8 transistors are OFF. Hence, pre-charged nodes start discharging through the tail transistor. The discharging rate depends on the inputs which are being placed on the input transistors T1 and T2. Suppose Vin1 > Vin2, then the OUT node is getting discharged faster than the OUTB node. This makes the OUT node to be discharged to 0 voltage (low voltage). The outputs are taken from a cross coupled latch section and the low output at OUT node pulls up the OUTB node to a high value. This conventional

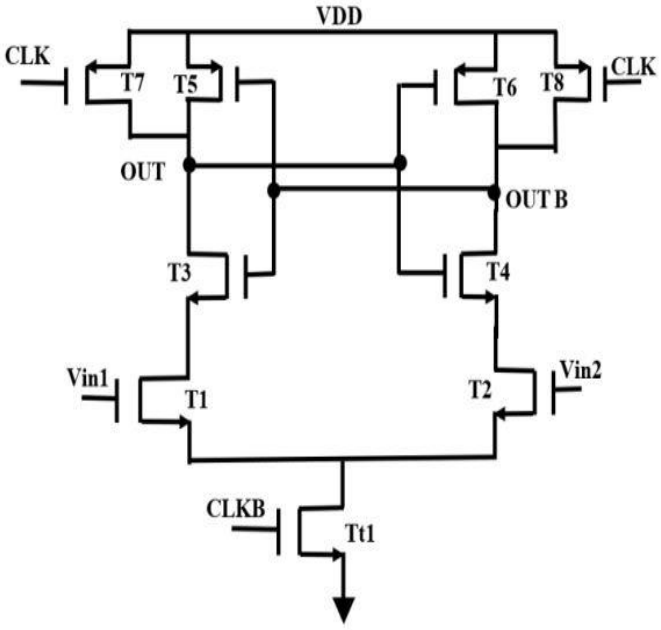

Fig. 3. Single Tail Comparator.

design is prone to many disadvantages. This comparator is having stacking transistor effect and large supply voltage is necessary for its operation. This would be a reason for power consumption. Secondly, kick back noise is a major concern. The noise in the output is coupled

to the input side and degrades the input. The comparators accuracy is compromised due to the kick back effect and offset voltage (it is due to threshold voltage variation). A double tail comparator with two stages of operation will solve these problems.

2.2 Two stage two-tail comparator

An existing two-stage, two- tail comparator is given in Fig.4. Tt1 and Tt2 transistors are the tail transistors. The Tt1 is a PMOS transistor which is used to provide a large current for strong positive feedback to the latching stage and the Tt2 (small NMOS) is used to provide a less current in the pre-amplification phase for reducing the offset effect. When CLK is low (CLK = 0), Tt1 and Tt2 are OFF. The low clock signal turns on TP3 and TP4. The pre-amp outputs are now charged up to 'Vdd' and these are used to drive the transistors T5 and T6 in the latching stage. This makes the outputs of the latching stage discharge to ground. This is the initial reset condition for comparator. In the evaluation phase, the CLK = is high (CLK = 1). Transistors Tt1 and Tt2 are ON and TP3 and TP4 are OFF. The Fp and Fn (outputs of the pre-amplification stage) discharges. The rate of discharge is proportional to the value of input signals which are being fed to the TP1 and TP2. A "ΔV" voltage is developed across the pre-amplification outputs. This is coupled to drive the latching stage. Accordingly, one output is pulled to Vdd (either OUT or OUT B) and the other is pulled to GND (positive feedback at latch makes it faster than the pre-amplifier). Stacking effect is reduced in this design. Hence, the circuit can work with low supply voltages.

The conventional design of dual tail comparator suffers by the following disadvantages. During decision making phase, the output voltage of the pre-

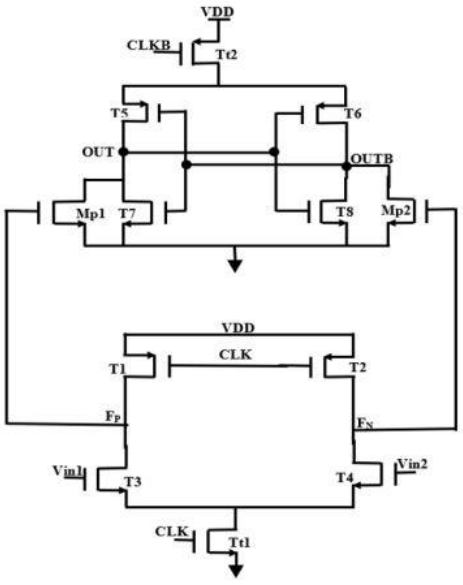

Fig. 4. Two-Tail dynamic Comparator.

amplification stage discharges from 1V to 0V. This charging /discharging activity continues after the latch stage is made its final decision. This brings about additional power consumption. Compensatory methods to reduce the power

consumption (additional control signals are required) results in increased delay and complexity. The other disadvantage is that the presence of transistor T5 and T6 increases the offset due to transistor mismatch and this contributes to reducing conversion accuracy

3.Proposed Dynamic Dual Tail comparator

The proposed comparator is shown in Fig.5.Here, the pre-amplification outputs are directly supplied to the sources of T9 and T10 . The input transistors in the regenerative latching section have been removed in the proposed design. The Tt1 tail transistor is removed from the design and two more transistors (TP1 and TP2) are added parallel to transistor T7 and T8 respectively.

The purpose of these newly added transistors is to drive the clock in the lath stage. The offset voltage effect and the transistor mismatch effects are minimized in the new technique. In the pre-amplification phase, the clock signal applied to drive T1 and T2 transistors are removed. The FN and FP nodes are connected with the gates of T1 and T2 respectively (cross-coupled). This is done to improve the pre-amplifier differential gain to speed-up the latching operation.

The operation of the proposed comparator involves two stages.

3.1 Operating Principle

The entire working can be sub-divided as:

• *Initial or Pre-charging stage*:

The CLK is made low (CLK = 0), then the transistor Tt1 is in the OFF state. The transistors TP1 and TP1 in the latch section are ON under this condition. The OUT and OUT B nodes are charged to high state (V_{dd}). The transistors T9 and T10 also get ON under this condition and the FN, FP nodes are charged up to supply. This is

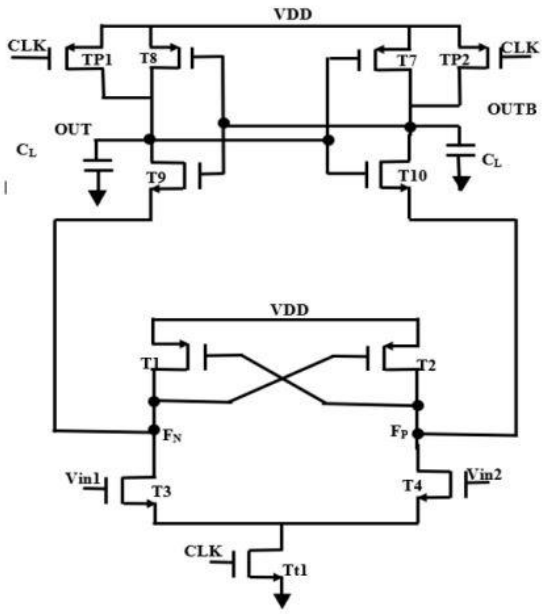

Fig. 5. Proposed Double Tail comparator.

considered as the initial state or pre-charged state of comparator.

• *Decision Making phase:*

To enter in the decision-making phase high signal is placed on clock terminal (CLK = 1). The transistor Tt1 is ON and outputs FN and FP discharge at different rates. The rate of discharge depends upon the input signals, which are applied for comparison. Suppose the input voltage Vin1 is greater than the Vin2 (Vin1 > Vin2). This makes the transistor T3 conducts faster than T4. As a result, FN starts discharging faster than FP. This allows the OUT node to discharge to GND. Transistor pair T8, T9 and T7, T10 are the cross-couple inverter arrangement in the latching phase. The low value at OUT switches on the transistor T7 and T10 gets switched off. This enables the OUTB node to charge to V_{DD}.As the evaluation phase is completed, OUT node is turned to low voltage (0V) and OUT B is turned to high voltage (V_{DD}).

Input transistors in the latching stage are removed in the new design. The absence of input transistors in the proposed system has certain advantages. This significantly improves the power efficiency. Since the transistor count is less in this design, the layout requires less area. This design offers less process variation and mismatch error compared to the conventional dynamic comparators and thus minimizes the offset voltage.

3.2 Delay Calculations

Delay performance of a comparator is having two components.

• Latching delay (T_{LATCH})

• Load capacitance charging delay (T_{OD})

The time taken by the cross coupled inverters to arrive at the final output is called as T_{LATCH}. T_{OD} is the time for charging the C_L , till the transistors T9 and T10 turn ON. Hence the delay can be expressed as:

$$T_{DELAY} = T_{OD} + T_{LATCH}$$

T_{OD} can be expressed as given in (1)

$$T_{OD} = \frac{V_{TN}}{I_{D1}} C_L \qquad (1)$$

$\boldsymbol{V_{TN}}$ is NMOS transistor's threshold. ID1, the drain current flows through T9. Current ID1 can be expressed in terms of the current through tail transistor T_{t1}/ ($I_{D1} = IT_t/2$). Now the equation (1) can be rewritten in terms of IT_t as:

$$T_{OD} = 2.\frac{V_{TN}}{IT_t} C_L \qquad (2)$$

Next, we need to find out the latching delay (T_{LATCH}). The relationship is shown in (3)

$$\frac{C_L}{gm_{eff}}.ln.\frac{\Delta V_{out}}{\Delta V_o} = \frac{C_L}{gm_{eff}}.ln.\frac{V_{DD}/2}{\Delta V_o} \qquad (3)$$

ΔV_{out} is the final differential output and it is taken as VDD/2. ΔVO is the initial voltage difference at the output terminals at time t = $\boldsymbol{T_{OD}}$ (This time indicates the start of latching operation). $\frac{V_{DD}}{2}$ is pulled up to the full rail voltage by the latching process. The term gm_{eff} indicates the inverter pairs effective transconductance. Considering the relationships shown in (1), the ΔV_o can be expressed as in (4).

$$\Delta V_o = OUTB(t = \boldsymbol{T_{OD}}) - OUT(t = T_{OD}) \qquad (4)$$

Using the Eq(1), the above equation can be rewritten as in (5).

$$\Delta V_o = V_{TN} - \frac{I_{D2}T_{OD}}{V_{TN}.C_L} \quad (5)$$

ID2 is the drain current flows through T10.From the circuit diagram (refer Fig.5), we can say that $I_{D1} = I_{D2} = IT_t/2$.

$$\Delta V_o = V_{TN} - (1 - \frac{I_{D1}}{I_{D2.}}) \quad (6)$$

In (6), the term ID2 –ID2 indicates the latching current difference and it is denoted as ΔID. The expression is given in (7).

$$\Delta I_{oD} = gm_{eff(9,10)} - \Delta V_{FN/FP} \quad (7)$$

$\Delta V_{FN/FP}$ is the differential voltage between F_N and F_P (at t = TOD). $gm_{eff(9,10)}$ is the transconductance of T9 and T10 transistors. Now ΔVO can be expressed in terms of ΔI_D and I_{D2} is represented as $\boldsymbol{IT_t/2}$.It is given in (8).

$$\Delta V_o = \frac{2V_{TN}.gm_{(9,10).}\Delta V_{FN/FP}}{I_{Tt}} \quad (8)$$

$\Delta V_{FN/FP}$ is found found using the following relationships (equations (9) and (10).

$$\Delta V_{FN/FP} = V_{FN}(t = T_{OD}) - V_{FP}(t = T_{OD}) \quad (9)$$

$$\Delta V_{FN/FP} = T_{OD}.\frac{I_{N1}-I_{N2}}{C_{L_{FN(FP)}}} \quad (10)$$

I_{N1} and I_{N2} are the current (discharging) flowing through the input transistors T3 and T4. The differential current is termed as ΔI_N and it is given in (11).

$$\Delta I_N = gm_{1,2}.\Delta V_{in} \quad (11)$$

$gm_{1,2}$ is the transconductance of T3 and T4. Eq. (10) and (11) are substituted in (8) to get the final expression for ΔV_o. It is given in (12).

$$\Delta V_o = (2V_{TN}/IT_t)^2.\frac{C_L}{C_{LFN(FP)}}.gm_{1,2}.gm_{9,10}.\Delta V_{in} \quad (12)$$

Now the total delay ($T_{DELAY} = T_{OD} + T_{LATCH}$) equation can be written as

$$T_{DELAY} = 2.\frac{V_{TN}}{IT_t}C_L + \frac{C_L}{gm_{eff}}ln.\frac{V_{DD}I_{Tt}^2C_{LFN(FP)}}{8.V_{TN}^2.C_L.gm_{9,10}.gm_{1,2}.\Delta V_{in}} \quad (13)$$

Following observations are made from (13).

The relationship shows a strong dependence of differential input voltage on the output differential voltage (initial condition). ITt(tail current) and transconductance of

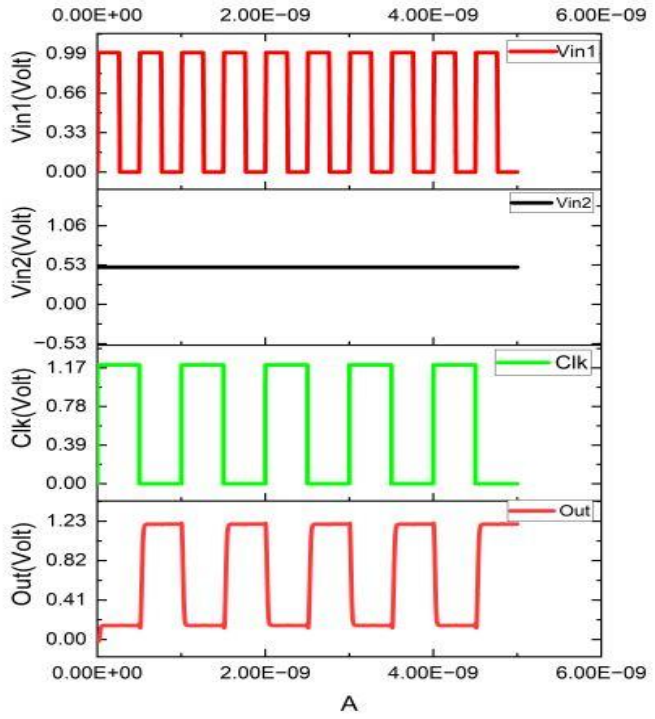

Fig. 6. Transient plot analysis performed at Vcm = 0.5V, VDD = 1.2Vand Clock = 1GHZ.

T3, T4, T9, T10 transistors also contribute to the performance of the comparator.

4. Results and Discussions

The circuit was designed and simulated in Cadence Virtuoso in 90nm technology. The inputs (Vin1, Vin2), Clock signal (Clk) and the comparator outputs (*Vout*) are plotted in Fig.6. Input signal 1(*Vin1*) is a pulse train of frequency 1GhZ.Input signal 2(*Vin2*) is a 500mV constant signal. A clock signal of 1GHz is used for this operation. A transient simulation of the proposed design was again performed with a sinusoidal signal. The Vcm of 0.5 V and a 1Ghz clock signal was used. The result of second simulation is shown in Fig.7.Average power consumed was found 12.98 µWatt. This power consumption is found as the lowest compared to the existing architectures shown in Table.1. The system given in [16] consumes 48.2µWatt power at Vcm of 0.5V. Power dissipation versus Vcm analysis for different *ΔVin* has been done (Fig.8).

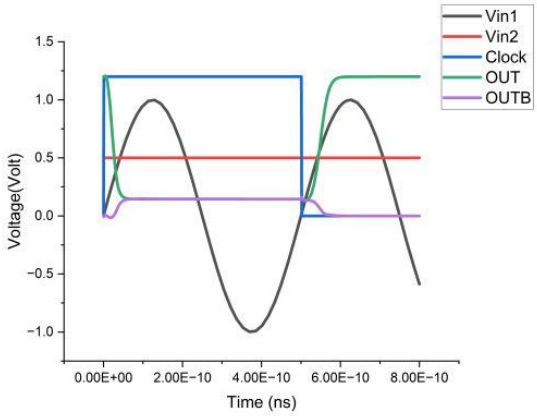

Fig. 7. Transient plot analysis performed at Vcm = 0.5V, VDD = 1.2Vand Clock = 1GHZ

It is seen that the proposed design only consumes 9 µ Watt power at Vcm = 0.4V. Thus, results show that, the new circuit outperforms other dynamic comparators in power efficiency.

The delay analysis was also performed using cadence tool. The circuit exhibits a

delay of 260ns, which is also a moderate number. The delay for different *ΔVin* against Vcm was plotted (Fig.9). When compared with

Table.1.

Papers	[4]	[18]	[14]	[19]	[15]	[20]	[16]	This work
Technology node(nm)	180	90	180	65	65	90	90	90
Supply(V)	1.8	1	1.2	1.2	1	1	1	1.2
Clock (GHz)	.5	1	.5	6	20	1	1	1
Delay(ns)	638.91	51.76	268.6	42.7	14.28	50.9	20.95	260
Power(µWatt)	347	32.62	72.2	381	67.8	31.8	48.23	12.98
Offset(mV)	7.78	7.7	7.3	3.87	4.45	7.7	2.44	1.33
No. of Transistors	15	13	13	13	16	12	18	11

Table 1. Performance Comparison

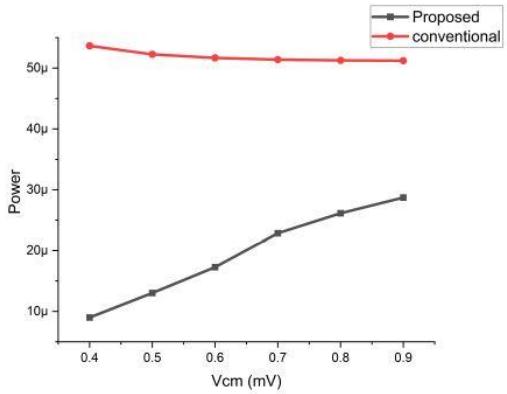

Fig. 8. Vcm Vs Power (for different Δ*Vin*).

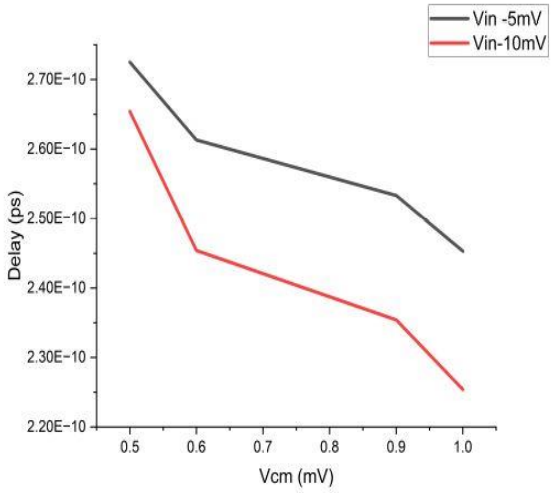

Fig. 9. Vcm Vs Delay (for different ΔVin).

Fig. 8. Vcm Vs Power (for different ΔVin).

existing design, this delay is high. In fact, in low frequency signal processing and acquisition (physiological signals), more than speed, reduction of power consumption is regarded as a predominant factor to increase the reliability of the system. The number of transistors (11 number of MOSFTs have only been used in this circuit) used is less, which makes the design simpler. Monte Carlo analysis of 250 run was performed on the proposed circuit to obtain the offset voltage.

The offset is found to be 1.33mV. Monte-carlo analysis is given in Fig.10. This is a better offset value compared to the existing designs. The data furnished in Table.1 justifies the improvement in offset voltage.

From the above-mentioned points, we can conclude that, this design would be a good candidate for the low power dynamic comparator for biomedical applications. Generally, if a low power technique is applied to a design, the speed and area characteristics deteriorate, but the proposed circuit improves the same.

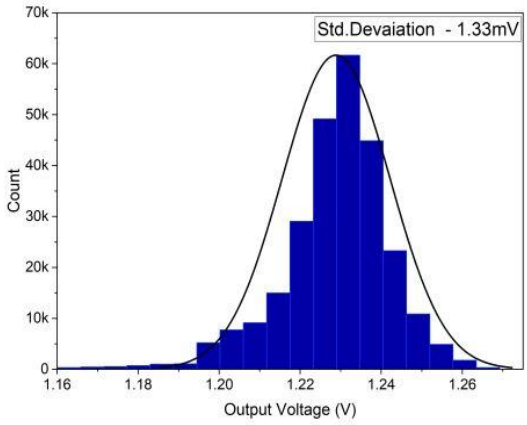

Fig. 10. Monte-Carlo result.

Fig. 10. Monte-Carlo result

5. Conclusion

An improvised design for two stage dynamic comparators for biomedical systems is proposed. This design irons out the power and offset problems pertaining to the conventional dynamic comparators. The first stage outputs are directly fed to the sources of NMOSFETs in the regenerative stage. The input driven transistors in the latch stage have been removed from the design. This concept helps to nullify the mismatch effect and in turn reduce the offset error. Moreover, the PMOS transistors in the first stage are back-to-back connected, and this increases the differential gain of the pre-amplifier and it speeds up the latch operation. Now a days, we are witnessing an increase in the use of implantable biomedical equipment. To increase the reliability and durability of these devices, it must be consuming the lowest possible power. Hence, the proposed system can be a good participant for low power dynamic comparator design.

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