Non linear window function associated memristor application for design of spiking neuron circuit

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Abstract: **We propose a design strategy based on memristors, adaptive nanodevices that are basically immune to variability. In a spiking neural network that performs unsupervised learning, memristors serve as synapses. Memristors alter their spike timing dependent plasticity in order to adapt and learn. A rule that resembles homeostasis is used to change the threshold of neurons. System-level simulations demonstrate that performance can be compared to that of conventional supervised networks of a comparable level of complexity. The robustness of the scheme, its unsupervised nature, and the potency of homeostasis are also demonstrated, demonstrating that the system can continue to function even when the various memristor parameters are significantly changed. Additionally, the network may alter in response to stimuli using various coding systems.**

keywords: memristor, window function, neuron, pattern recognition

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1. Introduction:

Microelectronics has long been predicted to undergo a revolution. Nanodevices offer innovative functions like memristivity and are compact and low power [1]. However, their less desirable characteristics—strong unpredictability and difficulty achieving an adequate yield—have made their introduction into actual products difficult. Architectures and design approaches with a true immunity to device variability and a high degree of fault tolerance would be necessary to fully realise the potential of nanoelectronics.

Boosting neural networks have a significant advantage over artificial systems because the brain, in particular, relies on erratic and unpredictable synapses and neurons [2]. Despite this, the brain has computing efficiency that is higher than that of artificial systems. Designs that promise cognitive computing and fault resistance have been made by integrating CMOS neurons and memristor synapses [3]–[10]. This study uses system simulations to give quantitative findings on computing performance and variability robustness. We demonstrate that the key to effective learning with exceptional memristor variable tolerance is a more straightforward spike timing dependent plasticity technique. Unsupervised learning is used, and a homeostatic process is involved.

We provide a description of the necessary technologies and architecture and do system-level simulations on the database [11] to demonstrate the effectiveness and resilience of the technique. A layer to label the outputs can be added to the system's first totally unsupervised layer, which uses a reduced version of spike timing dependent plasticity to extract features from the inputs (section III). The network achieves good tolerance to the fluctuation of different memristors' properties and performs favourably when compared to traditional, supervised networks with a comparable number of configurable parameters.

Technical background:

A number of classes of adaptable devices have appeared recently. Memristors (memristive devices) [1], resistive RAMs [12], and adaptive transistors like NOMFETs [13] and OG-CNTFETs [14] are the most well-known of these. Utilizing them as synapses in neuromorphic circuits is a novel strategy (electronic

circuits that work analogously to the brain). In particular, it has been suggested [8,[9],[15]] and experimentally demonstrated [4] that such devices could mimic a biological synaptic trait known as spike timing dependent plasticity (STDP) [16],[17]—a characteristic that is thought to be the basis for learning in the brain [18],[19]. A significant advancement in computing might come from a system made of CMOS neurons and nanoscale synapses, which could enable cognitive-type activities. Through programmes like the DARPA SyNAPSE programme in the United States or initiatives of a similar nature in Europe and Asia, this same concept is currently generating a lot of interest. Its sustainability has yet to be proven, though.

All of these technologies have a significant amount of variability, as was earlier stated [20],[21]. Though it is believed that the issue will become better as technology improves, this improvement won't be externally observable, especially when we scale down to really small scales where the devices are more subject to manufacturing process variations. Because of this, it is challenging to create systems that can benefit from their enhanced capabilities. This study sheds some light on some possible uses for this technology.

In the framework of nanotechnological implementations, there have been numerous recommendations for the use of changeable adaptive devices. The majority of the suggested architectures use state-based supervised neural networks [7] or programmable logic (FPGA type) [22, 23]. In the first strategy, error mapping and redundancy are used to control variability; in the second, supervised learning based on error gradient descent is used in a conventional neural network strategy.

Our method addresses the variability problem in nanodevices via unsupervised learning and asynchronous spiking neural networks. It is novel and was inspired by recent work in computational neuroscience and neural networks [24]–[27]. Numerous studies that have been published have employed this strategy. As was already indicated, there have been numerous recommendations to use memristive devices for STDP [8, [9], [15]]. We suggest a streamlined STDP structure in this study that, in our opinion, will be simpler to implement and allow for more organic learning. Furthermore, we suggest a homeostasic property for the neurons that has never been employed in this setting but is demonstrated to be crucial for the robustness of the approach. Memristors with STDP have already been demonstrated to facilitate receptive field creation using an unsupervised strategy that is compatible with variability and synchronous neurons [5]. Our study uses asynchronous designs, which are common in the neuromorphic field [28, 29], to complete learning on a shared dataset. Utilizing entirely digital designs is the final method for using memristors to facilitate learning in a variability-compatible manner [10]. As a result, more hardware is needed per synapses [3]. In this article, we demonstrate how employing nanodevices with continuous conductance variation, variation tolerance may be maintained.

Network And Its Implementation Are Presented:

A. Architecture:

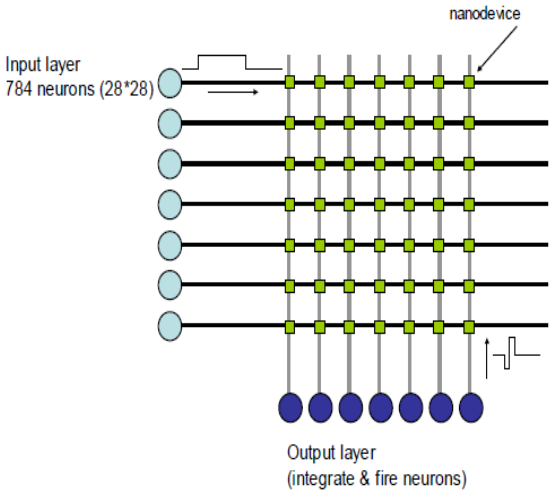

Figure 1: The topology of a circuit. The CMOS input layer and the CMOS output layer are represented by horizontal black cables (vertical grey wires). Adaptive nanodevices are located at the intersection of the horizontal and vertical wires.

In this study, we initially suggest a straightforward two-layer construction. I/O CMOS neurons are linked

by nanodevices called synapses in a feed-forward manner with a crossbar structure (described below). A compressed STDP protocol is used to teach the synapses (II.B.1). The output neurons exhibit a homeostatic trait and leaky integrate-and-fire behaviour (II.B.2) (II.B.4). Additionally, they are related through blocking linkages created by diffuser networks (II.B.3)

Numerous potential coding strategies, as detailed in section III, are used by the input neurons to send the stimuli as asynchronous voltage spikes (The relationship between spiking rate and stimulus strength). For example, the neuromorphic society may have developed a cochlea or spiking retina that directly causes these feelings [30, 31]. It is logical to arrange the nanodevices in the whole crossbar depicted in Fig. 1. The squares represent the nanodevices, while the dots represent CMOS silicon neurons and the synaptic driving circuits they are connected to. In actuality, synapses serve as tunable resistors. The crossbar arrangement enables the output to receive the whole current flowing through all of the synapses when several synapses are active simultaneously (i.e., receiving spikes). The setup of the system could possibly be more advanced. CMOL architecture, in which a crossbar of nanodevices is built on top of CMOS driving circuits and neurons [7]. As a result of learning, the output neurons will develop selectivity to particular properties included in the input patterns, making them more responsive to the numerous stimuli classes that are provided in an entirely unsupervised manner. The crossbar architecture cannot be implemented until the learning rule of the nano devices is totally local. The neurons' behaviour must be straightforward and simple to implement in a constrained area. We will now discuss how to do this.

B. Neurons and synapses

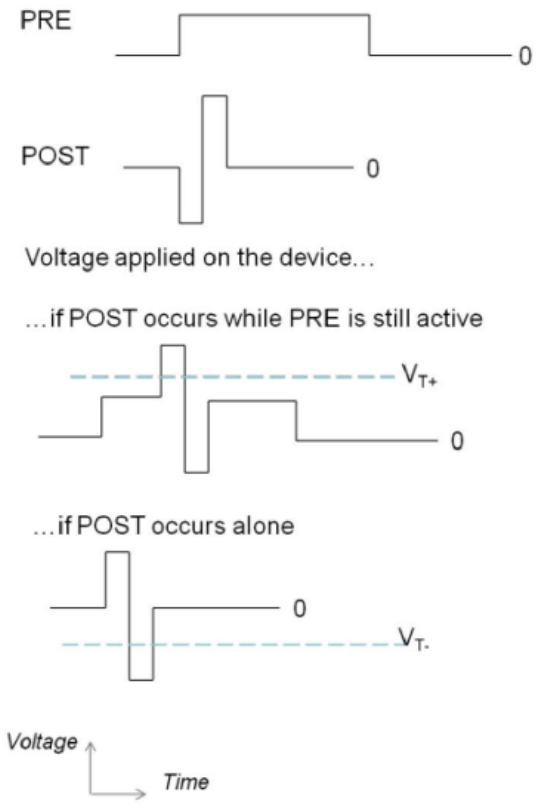

Figure 2. Pulses for an efficient STDP (voltage pulses as a function of time).

When an input neuron spikes, a PRE pulse is transmitted to the nanodevices connected to it. When an output neuron spikes, a POST spike is applied to the linked nanodevices. When the applied voltage (the difference between the voltages applied at the two ends) contacts VT+ or VT-, the device's conductance changes, correspondingly.

1) Synaptic activity Synapses function in this system in one of two separate ways. Due to the fact that they are variable resistors, they transmit pulses with varying conductance (or weight). The foundation for the system's learning is laid by the fact that they likewise alter their weight in response to the activity of the neurons to which they are linked.

These instructions are used to programme the memristive nanodevices. They become more conductive when a positive voltage pulse is applied that is higher than the VT+ threshold. They lose conductance when a voltage pulse is supplied that is

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below the negative threshold VT- [4], [8]. Memristors can implement spike timing dependent plasticity (STDP), a learning principle used by synapses in the brain, according to earlier research. In a publication similar to [8], [9], this was proposed, and [4] provided empirical evidence for it. We suggest a simpler modification to existing systems (Fig. 2).

• An input neuron spikes when it sends a lengthy pulse to a synaptic junction (PRE pulse). The memristor can receive a small amount of current from this voltage, but not enough to reprogram it. The output neurons integrate this current (resistor role of the synapse). When numerous synapses attached to the same output neuron activate at once, currents are pooled.

• A spiked output neuron emits pulses that alternate between a positive and a negative bias (POST pulse). In the absence of any PRE pulse, just the second component of the device crosses a threshold, lowering the synapse weight by w. As demonstrated in Fig. 2, the voltage provided to the device actually makes it heavier by w+ if the input neuron had just spiked and the PRE pulse was still being applied to the other end of the device.

This simple learning concept, the foundation of all learning is cognition, which nanodevices make simple to use. There is no requirement for delay matching between the PRE and POST synaptic waves, which should make developing the driving circuitry much simpler than the fully bioinspired and more complicated technique provided in [9]. Additionally, our feed-forward implementation is better suited to the learning rule.

This key concept for learning functions in a clear and understandable manner. The synapses linked to previously spiking input neurons have their weights boosted by w+ when an output neuron declares a spike (at time tspike) (from tspike to tspike-tPRE, if tPRE is the duration of the PRE pulse). All of its other synapses' weights are decreased by w. This increases the neuron's sensitivity to the specific pattern that initially stimulated it and raises the possibility that it will spike in response to another occurrence of that pattern. This strategy, which we show in this research works remarkably well in practise, has been conceptualised in some degree in [27].

In our system simulations, we simulate the weight increases and decrements w+ and w using the memristor with new window function from [4],[32]. When a POST happens: In the event that a PRE It took place right before the weight was increased by

$$\delta w_+ = \alpha_+ e^{-\beta_+ \frac{w - w_{min}}{w_{max} - w_{min}}}$$

in the other cases it is decreased by

$$\delta w_- = \alpha_- e^{-\beta_- \frac{w_{max} - w}{w_{max} - w_{min}}}$$

The exponential factor shows that applying the same voltage pulse repeatedly to most memory technology has been found to have a lower impact on the conductivity of the device [4],[32]. This typical (partially multiplicative) device activity is helpful for learning. The selected PRE and POST pulse voltages have a substantial influence on the parameters +, -, +, +, and +. Device variability may affect these figures as well as the minimum and maximum weights, wmin and wmax.

2) Output neuron dynamics: For the devices to be used to their full potential, they must be connected to silicon neurons, which are processing units that can integrate their input, process it, and produce spikes in a bio-inspired manner. The usage of analogue circuits with transistors that typically function in the sub-threshold zone and are capable of receiving and producing asynchronous spikes is a well-researched technique in the field of neuromorphics [28, 29]. Variability is still a significant issue for such devices, while being less severe than in nanodevices. This challenge [31] is faced by any neuromorphic design, and it will only get more challenging as technology advances.

The fundamental equation is designed to be solved by leaky integrate-and-fire neurons (expressed in normalised unit):

$$\tau \frac{dV}{dt} + gV = I_{input}$$

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where V represents the neuron's state variable (current or voltage). Iinput is the amount of current flowing through the neuron's crossbar line:

$$I_{input} = \sum_{j} I_j$$

where Ij denotes the flow of current across every output neuron-connected memristor j.

The integration is halted for a period of time known as the refractory period when V reaches a particular threshold, Vth, at which point V is reset to zero.

These neurons have been built using either neuromorphic circuits with positive feedback, like those in [28, [29], or compact CMOS neuromorphic circuits, like those in [33].

This sort of CMOS device uses incredibly little power since the subthreshold zone is where most transistors work. and because asynchronous processing is employed [28],[29]. However, nanotechnology will have a significant impact on the power needs of the nanosynapses, and those needs should go up as the devices get bigger.

The spiked output neurons should provide the layer's other output neurons get inhibitory signals that stop them from firing during the inhibition period and reset their potential to 0.

Using diffuser networks, as in [28], it is possible to effectively produce this inhibition between the neurons. The network resembles a Winner-Takes-All topology as a result of this inhibition [27].

More particular, the state variable V of the other output neurons is reset to zero when an output neuron spikes during a time inhibitor.

4) Homeostasis: The architecture's final difficulty is modifying the neurons' threshold. Despite the fact that it is required, this is not the case for spiking neurons even though it is normal for traditional artificial neuron networks. Using a revolutionary strategy called homoeostasis, which was inspired by biology [2], the neurons generate a goal activity (i.e. a number of times an output neuron should spike over an extended period of time, like 100 digits presentation). If the neuron's average activity is higher than the target, the threshold is consistently raised; if it is lower, the threshold is reduced..

The thresholds of the neurons to the stimuli for which they have developed a specialisation are altered as a result, ensuring that all of the neurons' outputs are utilised. In neuromorphic circuitry, homoeostasis has been achieved using analogue memories, as demonstrated in [34], or it could be accomplished digitally.

Results: For the memristor output in this work, a new window function was taken into consideration. The development of a circuit for spiking neurons uses a memristor with a proposed window function. The outcomes are contrasted with the Joglekar and Biolek window function, a traditional window function. A two-layer thin TiO2 film (size D 10 nm) sandwiched between platinum contacts makes up the physical model of the memristor:

$$0< x=w/D <1$$

The variable w (width) varies from 0 to 1.

According to the Joglekar window function [3]:

$$F(x) = 1 - (2x-1)^{2p}$$

where p is an positive integer. It determines the models behavior in linear or in nonlinear drift disappear as it increases. Biolek proposed another window function [4] ,introduced a current parameter *I* along with the variable *m* and *p* which are related as:

$$F(x,i) = 1 - [x - stp(-i)]^{2p}$$

The proposed window function equation is given as:

$$F(x) = j\{1 - [(sqrt(x) - 0.5)^2 + 0.75]^{4p}\}$$

using the above mentioned window function the memristor V-I characteristics are simulated. The graphs is generated for comparing the Biolek and Joglekar window functions for different p-values with proposed window function.

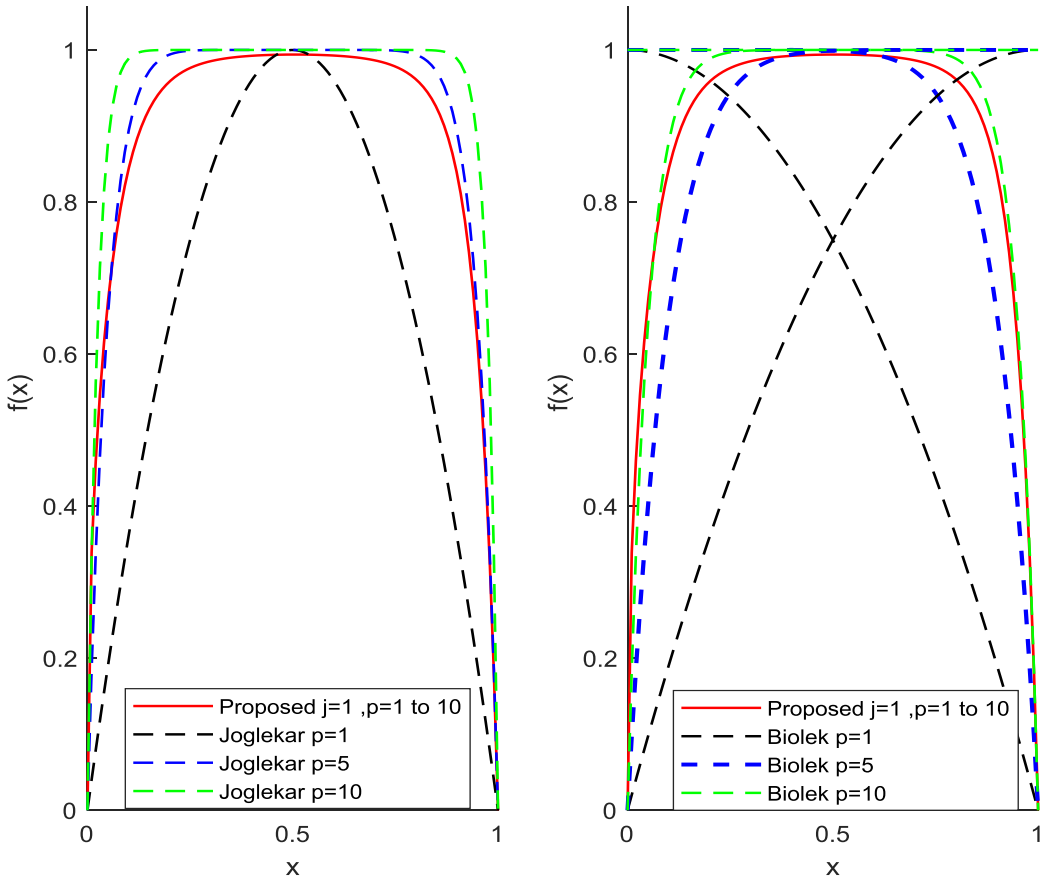

Figure 3: The window function plot for Joglekar window function and proposed window functions (left) and the graph of Biolek window function with proposed window function (right).

In the figure 3 the propose window function f(x) characteristics are shown with respect to x ate different value of parameter p. The variable x varies as the un doped region width is varies from 0 to D. In this graph the p value varies from 1,5 and 10 for Joglekar (Left) and Biolek (right) window while for the proposed window function the p is piecewise varying with c from 1 to 10.The non linearity drift parameter j is taken to be 1.

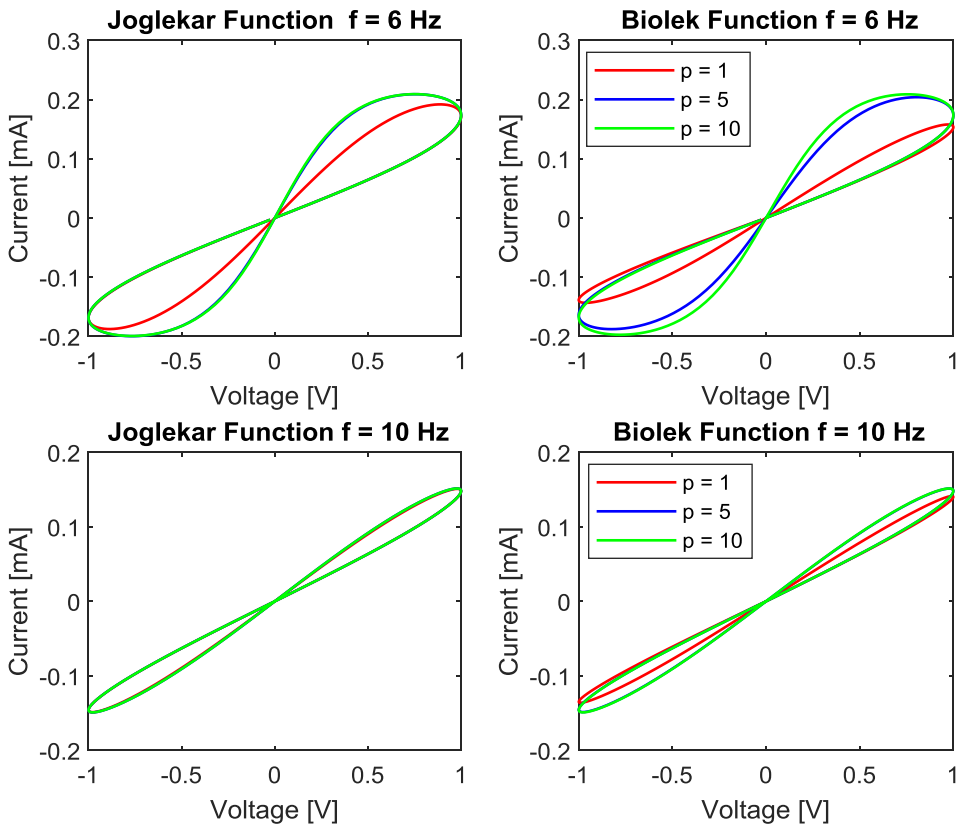

Figure 4 a:V-I characteristics for Joglekar (Left) and Biolek (Right) window function at voltage supply frequency f= 6Hz (top) and f=10Hz (bottom).

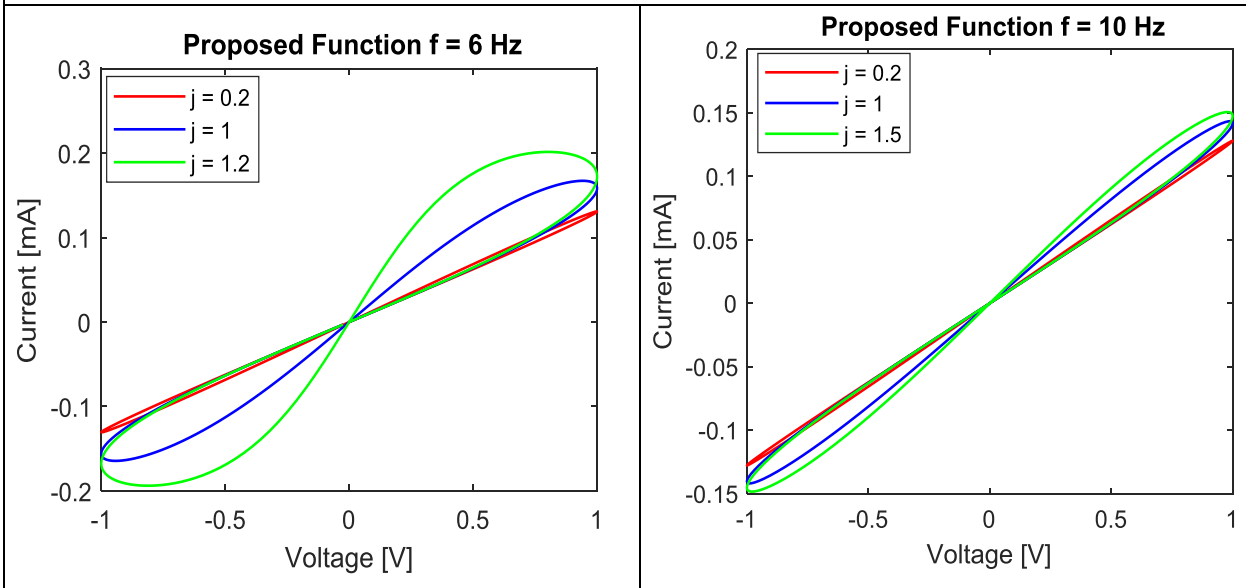

Figure 4 b:V-I characteristics for proposed window function at voltage supply frequency f= 6Hz (left) and f=10Hz (right).

Figure 4a and 4b shows the V-I characteristics for the memristor with Joglekar/Biolek window function (figure 4a) and Biolek window function 4(b) at two different input voltage supply frequency of 6Hz and 10Hz.As the frequency increases the curve is shrinks towards the centre.

The script is simulated for the convergence of a neuron with memristor non-linear for different values of p using the proposed window functions. The results are compared in graphs. The percentage detection error of given patterns is taken as performance parameter for training the neural network model. Figure 5 a, b and c shows the training response of simulated NN circuit using spiking neuron designed from window function based three different memristor.

Figure 5 a shows the convergence plot during NN model development using Joglekar window function based memristor. The y axis shows the percent detection error and x axis are number of epochs. As the epochs increases the error is reducing. In 650 (approx.) epochs the error reaches to zero. Similarly in figure 5b and 5c the the error converges to zero at 600 epoch number and 550 epoch number. Hence it shows that our proposed window function based memristor application in spiking neuron models has faster learning rate as compared to conventional window functions.

The figure shows the symbolic block based representation of showing the memristor based neuron as a device. In this neuron device two trigger pulses are associated for reset and read signal input. As the reset or read input are given the switch goes on and input voltage level of Vreset or Vread is acknowledged at the positive port terminal of memristor device. The voltage at the memristor is collected as the storage buffer. In the condition of different input selection like Vread,Vreset or Vwrite output pulses are generated at different pulse width as shown in the figure 6 (b).

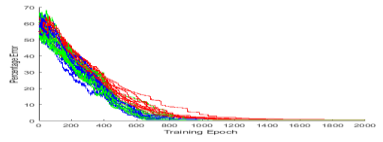

Figure 5a: Training performance of NN model for memristor with Joglekar window function.

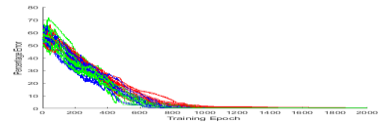

Figure 5b: Training performance of NN model for memristor with Biolek window function.

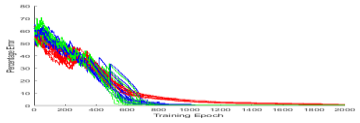

Figure 5c: Training performance of NN model for memristor with proposed non linear window function.

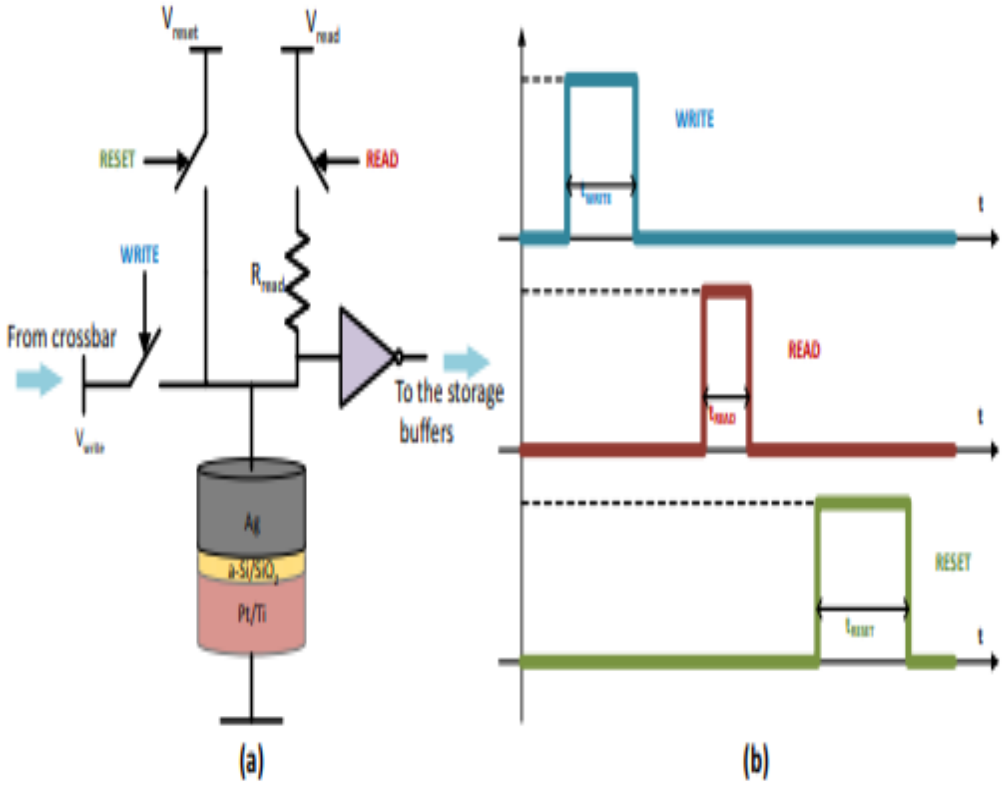

Figure 6(a) : Representation of memristor based neuron circuit. (b) The read,write and reset input based temporal response for control signal in a single step time.

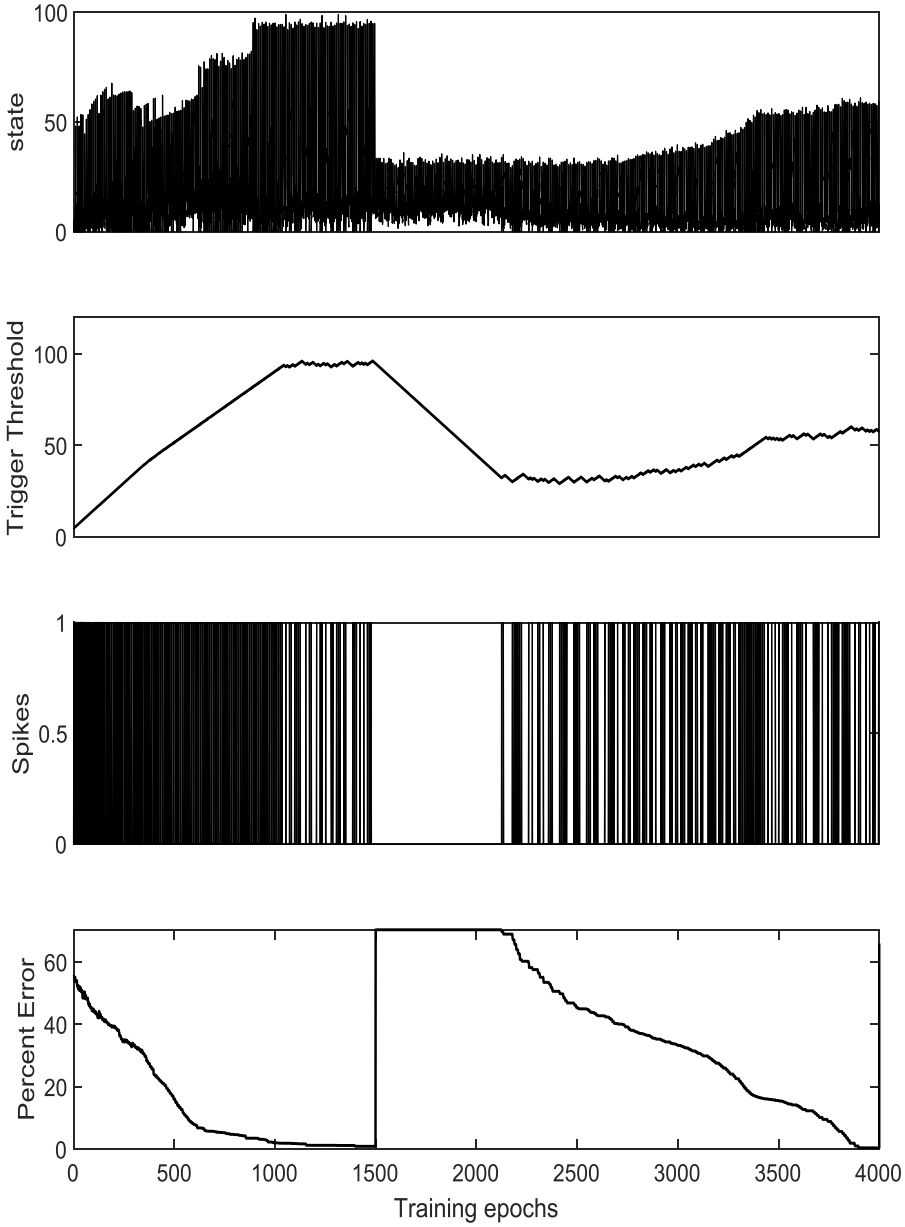

Figure 7: (a) State transition of neuron response with respect to time. (b) Variation in the trigger threshold with respect to time (c) Spikes generated at the neuron mode of memristor with proposed window function.(d) Percent error at different epoch with respect to variation in the threshold.

The neural network developed using the proposed window function based memristor circuit is trained for different input pateern. The neuron states are changed from reset ,read to write state as shown in figure 7(a) and the trigger threshold is varied under the different training epochs as shown in figure 7(b).Different neuron spikes

patterns are generated as shown in figure 7(c) and the training is finally converged at zero value of percent error at near about 4000 epochs.

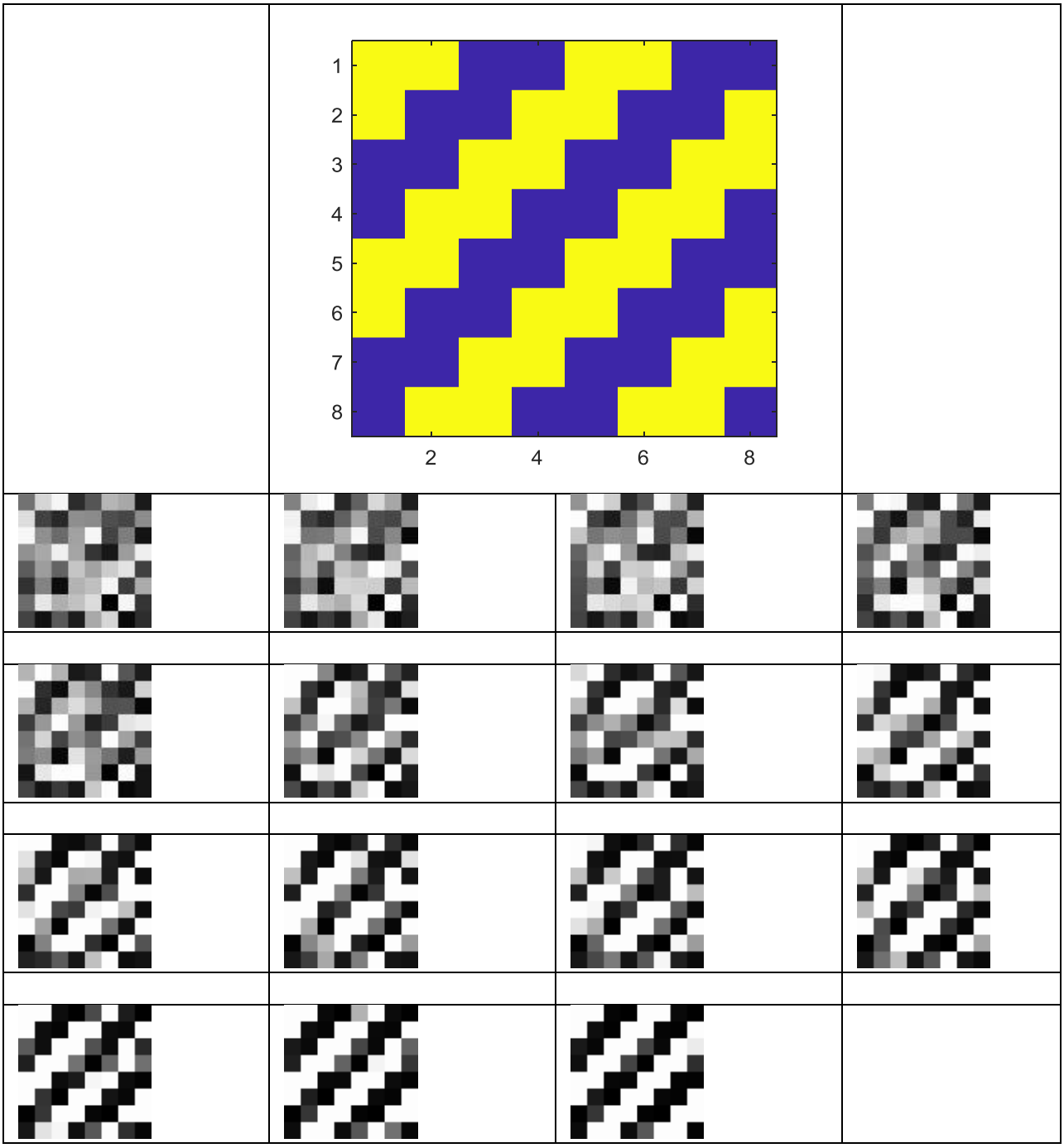

Figure 8: Pattern recognition step by step progress representation using proposed window function based memristor circuit of neuron.

Conclusion:

In this research, we demonstrate how to do unsupervised learning in a very variability-resistant manner utilising basic memristors connected to window function circuits. The basis for this tolerance and the system's exceptional adaptability is nonsupervision. Also mentioned as a crucial element to maintain insensitivity to signal fluctuation is homeostasis. A second-layer memristor-based method for supervised learning was also introduced in the previous section. When used to label the output of the first unsupervised layer, it maintains high variability robustness and provides a way for fully learning real-world case data. Future circuits that efficiently and compactly process natural data may be built on the basis of this design concept. These circuits' capacity for unsupervised learning will enable them to adapt to a variety of environments. Future studies should focus on experimentally proving these concepts and demonstrating how they can be scaled to increasingly complex multi-layer networks and a variety of sensory stimuli.

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