Performance Based Study: RLG Based Decoder For qALU Using QCA Designer Tool

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Abstract—

The size in terms of area of the chip with reversible logic technique has received significant significance in the new years in light of its component of reduction in power in terms of heat dissipation that enhances the life span of the device. Because of this ample examination, it has been happening with encoding and interpreting circuits utilizing reversible concept-based approach. The decoders are the main circuits utilized in combinational problems that shapes the premise of the handling of the qALUs of the quantum processors. However, it has been also observed that these decoding modules of the processor consumes substantial amounts of power during the execution of the task. Thus, there are two basic issues with this system that needs to be targeted i.e., loss of power because of heat and power dissipation in the circuits of the decoding system of the processor. In this discussion, the author has put forward certain techniques which will resolve this limitation of the circuit with the proper use of the RLGs that will in turn enhance the overall power consumption of the system. In this paper, an innovative approach has been made for the designing of a novel 2:4 & 3:8 decoders with the use of RLGs and QCA Designer Tool 2.0.3. The operational based discussion of decoder has been put forward and a formerly existing plan and numerical assessment of the quantum cost for and inputs decoder has been discussed in this article.

Keywords-Reversible Logic, Quantum Computation, QCADesigner, Delay Period, Decoder, Quantum Cost.

DOI Number: 10.4704/nq.2022.20.14. NQ880171 **Neuroquantology 2022; 20(14):1264-1270**

I. INTRODUCTION

In Very Large-Scale Integrated Circuits (VLSI), the circuit-based problems are contracting dramatically thus, the circuit behavior is developing dramatically with complications. Further, the modeling of the tool with scaling is restricted by the power dissemination, requiring better power strategies. As per Rolf Landauer, heat produced because of the deficiency of the slightest bit of data during calculation is about KTln2 in joules where K is the Boltzmann consistent and T is the outright temperature at which calculation is performed. Since in reversible circuits the quantity of piece misfortune is there subsequently preferably in reversible circuits no influence dispersal happens. In any case, basically, some power scattering do happen, which is substantially less than the customary rationale. In the present time, the need of reversible registering can't be disregarded. Reversible calculation can be acted in a framework just when the framework contains reversible circuits. A quantum PC will be seen as a quantum organization (or a group of quantum organizations) made out of quantum rationale doors; It has applications in different exploration regions like Low Power Complementary Metal Oxide Semiconductor (LPCMOS) plan, quantum processing, nanotechnology, DNA Computing. Reversible circuits are those circuits, which have balanced planning among info and result vectors. A circuit is supposed to be reversible in the event that the information vector can be extraordinarily recuperated from the result vector and there is a coordinated correspondence to protect data during calculation. With the progress in innovation, the tool aspects are contracting dramatically thus the circuit intricacy is developing dramatically. After specific guide the gadget scaling is confined due toward power dissemination, which has made interest in research area of Reversible Logic circuits. As per Rolf Landauer, heat created

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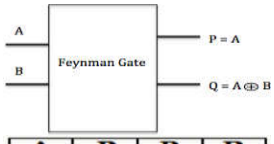
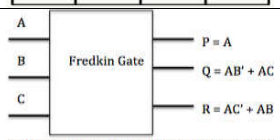
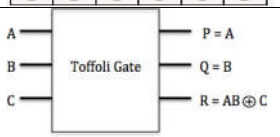
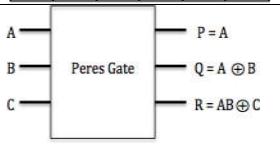
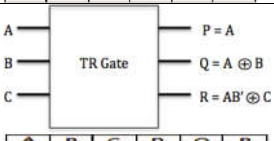
Relevant conflicts of interest/financial disclosures: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

because of the deficiency of the slightest bit of data during calculation is about KTln2 in joules where K is the Boltzmann consistent and T is the outright temperature at which calculation is performed. Bennett proposed an answer for the issue of intensity dispersal [01-05].

In this conversation, we have introduced the fundamental thoughts on the execution boundaries which decides the problem and execution of circuits and a few famous reversible logic based issues. The principal motivations behind planning reversible concept are to diminish quantum cost, smartness of the circuits, the quantity of trash yields, consistent sources of info, region and power. Decrease of these boundaries is the level of the work engaged with planning a reversible circuit are Quantum Cost, Garbage Output, Constant Input, Area and Power, Delay, Fault Tolerance Gates, Reversible Logic Gates, Fan In, Fan Out [06-10].

TABLE I. REVERSIBLE LOGIC GATES WITH THEIR DESCRIPTIONS [11]

Reversible Gate	***Description***	***Block Diagram***
Feynman Gate	FG as 2x2 RLG with the mapping (A, B) to (P, Q) with quantum cost value 1	 A B P R 0 0 0 0 0 1 0 1 1 0 1 1 1 1 1 0
Fredkin Gate	FRG a 3x3 RLG with the mapping (A, B, C) to (P, Q, R) with quantum cost is 5	 A B C P Q R 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 0 0 1 0 0 1 0 1 1 1 0 1 1 0 1 0 1 1 1 1 1 1 1
Toffoli Gate	TG a 3x3 RLG with the mapping maps (A, B, C) to (P, Q, R) with quantum cost 5. .	 A B C P Q R 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 0 0 1 0 0 1 0 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1 0
Peres Gate	PG a 3X3 RLG with the mapping between the inputs and the outputs as (A, B, C) to (P, Q, R, S) having quantum cost 4.	 A B C P Q R 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 0 0 1 1 0 1 0 1 1 1 1 1 1 0 1 0 1 1 1 1 1 0 0
TR Gate	TR Gate is a 3x3 reversible gate with quantum cost as 4.	 A B C P Q R 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 0 0 1 1 1 1 0 1 1 1 0 1 1 0 1 0 0 1 1 1 1 0 1

II. Basics of the Decoder circuit Operation

The equipment of computerized correspond-dence frameworks depends intensely on decoders as it recovers data from coded yield. The below given figure 1 shows the block system of 2:4 decoder, which can appear as a more than one input, more than one logic based output circuit that converts coded inputs into coded yields, where the info and result codes are unique. The traditional 2-to-4 reversible decoder requires just a single logical concept with no trash yield which has 7 quantum cost [12-15].

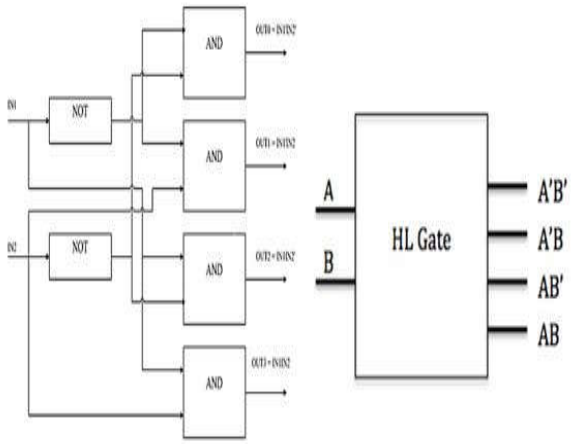


Figure 1. Basic & Conventional RLG Based 2-To-4 Decoder [16]

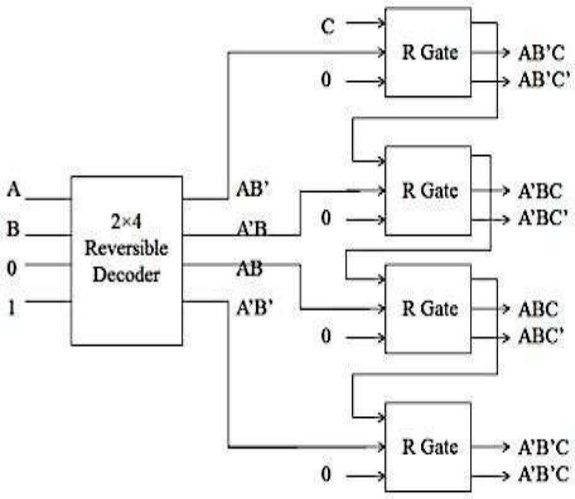


Figure 2. Efficient approach for 3-to-8 decoder using HL gate and R gate [16]

The circuit configuration has a similar micro circuit, trash results and the time taken by the circuit to process the output with further modified quantum cost. A reversible 3-to-8 decoder can be planned to utilize one 2-to-4 reversible decoder and four R logic circuit. R is a 3x3 reversible entryway having inputs (A, B, C) and results P = A; Q = AB and R = A'B + AC. The accomplishment of the plan of 3-to-8 reversible decoder plans was more noteworthy as the current best as far as quantum cost and deferral. Quantum cost of 3-to-8 reversible decoder utilizing R circuits is 23 when looked at by utilizing FRG Gate which is around 27. Fig. 2 shows graph of 3-to-8 decoder utilizing HL and R Gates [17-20].

The component level modeling of the CPU comprising of CU unit, ALU and Register documents and different parts which assumes a significant part in carrying out the entire execution of the task. Control Unit coordinates the activity inside the PC processor by coordinating the data sources and results of PC framework. Significant block of control unit is decoder, which is utilized to control the memory parts of processor assumes a widely significant part in presentation of by and large CPU. Subsequently, it will be on the right track assuming we say the guidance set decoder consumes more power. Consequently, by enhancing the level of the input of this unit will be useful to lessen the general power utilization of the framework. As indicated by this overview, the specialists have previously proposed reversible plans of numerous normal number juggling and coherent units, including adders, multipliers, shifters and even registers and other reversible part. Very little engaged work has been done explicitly on reversible decoder plan. A Decoder is a central structure block in many processing frameworks. To discuss the behavior of a decoder, firstly, we plan for a reversible 2-to-4 decoder, which has been utilized so as to develop a 3-to-8 decoder, etc. A 2-to-4 decoder should provide the out combinations with A'B', A'B, AB', AB, This discussion provide a quantum cost no less than multiple times the quantum cost of a solitary reversible AND capability doesn't give better execution. [21-27].

III. Analysis And Scope of the Proposed Model of the Decoder Circuit

The people involved in this domain discovers various reason because of which work has not been completed so as to decrease the quantum cost, retard time of the output, area and power which motivates to carryout further work that should be possible to lessen these boundaries. The implementation of the 3-to-8 reversible decoder was more prominent with the current

one yet configuration isn't abundantly streamlined regarding other execution boundaries. We can utilize the energy recuperation technique, which involves reversible rationale for power improvement. Additionally further work should be possible by reproducing the circuit on plan designer to obtain more precise outcome with respect to control utilization. Comprehensive hunt strategy ought to be utilized to find the reversible entryway with ideal arrangement, which creates the base quantum cost. Trash yields (yields which are not utilized) ought to be kept as least as could really be expected. Lessening the quantity of trash yields is one of the fundamental undertaking while at the same time utilizing reversible logic concepts.

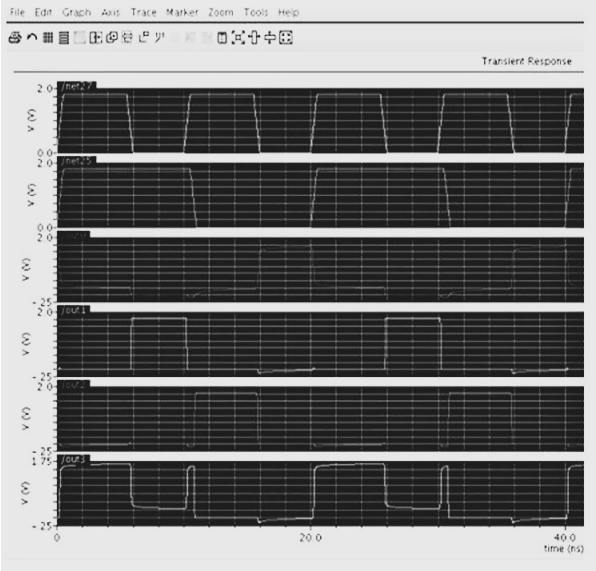


Figure 3. Simulation results of a conventional 2x4 decoder.

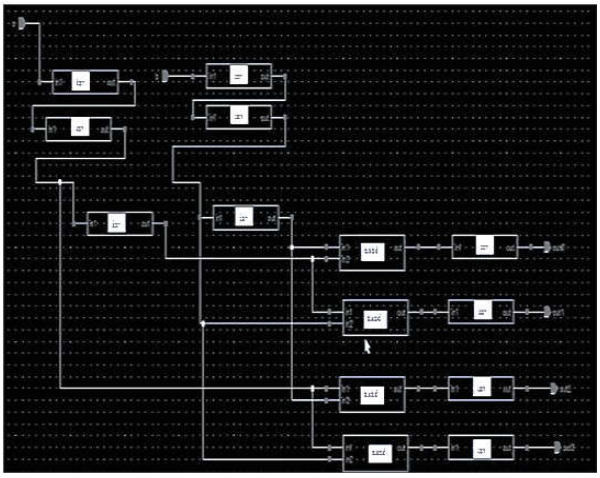


Figure 4. Conventional 2x4 Decoder.

A Conventional Decoder schematic diagram has been displayed in the figure 5. The circuit of a 2x4 Conventional decoder requires 2 BUFFERS (2 inverters associated in series frames a BUFFER), 2 INVERTERS and 4 AND (NAND gets followed by an inverter is an AND) logical based problem. Static power existing in the circuit is 2.298 micro watts. All out power scattered when the circuit is reconsidered for 80ns is 7.891 micro watts. Subsequently, the all output power disseminated through a traditional 2x4 decoder is 5.593 micro watts dismissing the power dispersal because of spillage flows. The decoder proposed in is built utilizing just Fredkin doors and is as displayed in Figure 5.

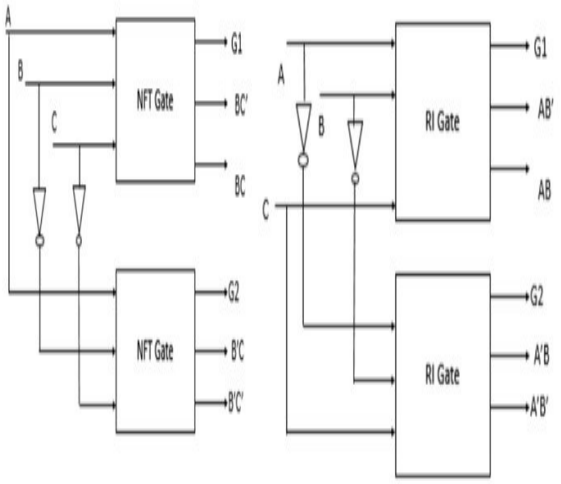


Figure 5. Schematic arrangement of Reversible Gates

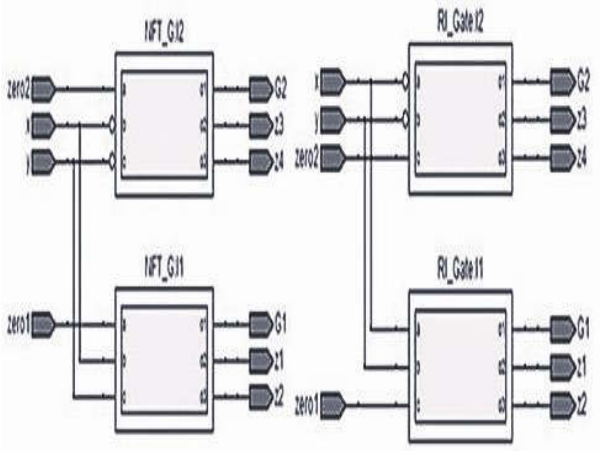


Figure 6. RLG Configurations Using NFT Reversible Logic Gates

The gate simulations of the proposed decoders are shown using QUARTUS II 9.1 Modelsim. The RTL diagram of 2:4 Decoder using NFT and R-I Gate is shown in above figures. Both designs use 2 gates each. Fig. 10 shows 2:4 Decoder using NFT Gate and Fig. 11 shows 2:4 Decoder using R-I Gate. Simulation results for NFT and

R-I Gate 2:4 Decoder. As seen in the result for different combination of X, Y input one of the output Z1, Z2,Z3, Z4 is high.

TABLE II. COMPARISON OF IMPORTANT MODELED PARAMETERS OF PROPOSED 2:4 DECODER CIRCUIT

2:4 Decoder Ref.	*No of Gates*	*Garbage Output*	*Quantum Cost*	*Constant Input*	*Reversible Logic Gate*
[15]	6	4	12	6	2 FG, 4 TG
[13]	4	1	12	2	2 FG, 2 FRG
[14]	5	1	11	3	1 PG, 1 TR, 3CNOT
[5,6]	3	2	12	4	1 F2G, 2 FRG
[12]	3	2	15	3	3 FRG
[11]	3	1	11	3	1 FG, 2 FRG
[3]	4	0	7	2	1 PG, 3 CNOT
[10]	1	0	8	2	1 FRG & Minimal reversible logic
[16]	1	0	7	2	HL Gate
Proposed	1	0	7	2	HL Gate

TABLE III. COMPARISON OF IMPORTANT MODELED PARAMETERS OF PROPOSED 3:8 DECODER CIRCUIT

3:8 Decoder Ref.	*No of Gates*	*Garbage Output*	*Quantum Cost*	*Constant Input*
[15]	10	4	32	-
[13]	12	2	36	6
[14]	8	16	32	7
[5,6]	7	3	32	8
[12]	7	3	35	7
[11]	5	10	28	6
[3]	7	2	31	7
[10]	8	1	27	6
[16]	5	1	27	6
Proposed	5	1	23	6

IV. SIMULATION RESULTA & DISCUSSION

The relative investigation between the decoder in [13] and the proposed decoder shows an improvement in quantum cost, line cost and trash yields. The quantum cost (QC) of the proposed decoder is 23 while that of referred is 32, No of Gates used for the proposed model is 5 while that of referred and similarly, we have got appreciable parameters as shown in Table 2, 3 and 4. Based on the comparative discussion of the proposed and referred work published by other researchers, the author may submit that these two RLG based decoder circuits provide the acceptable output that can be utilized in the design and implementation of the qALU.

TABLE IV. COMPARISON OF PROPOSED MODEL

	GC	*QC*	*TC*	*LC*	*GC*	*CI*
In [12]	3	15	24	6	1	4
Proposed Decoder	3	11	24	5	2	3

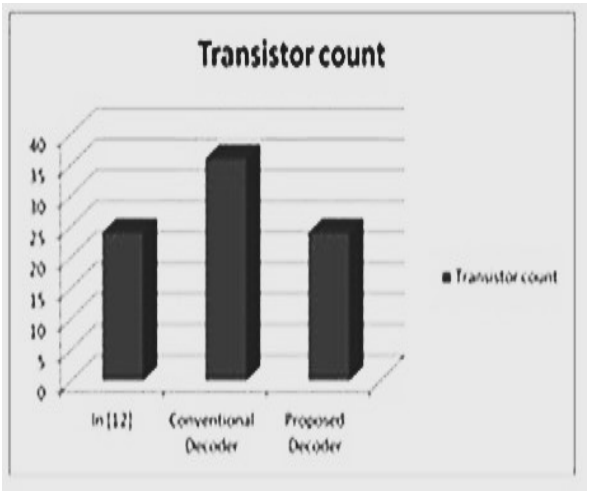


Figure 7. Transistor Count of the Circuit

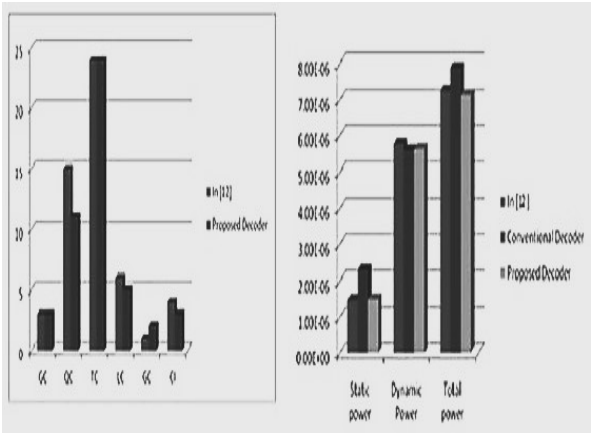


Figure 8. Comparison of dominant parameters of the proposed decoder

It is clear that the proposed plan has an improvement of 20% as far as quantum cost, 16.66% as far as line cost and half as far as trash yields. Figure 8 and 9 shows the diagram addressing something similar. It is apparent that the proposed plan has an improvement of 20% as far as quantum cost, 16.66% as far as line cost and half as far as trash yields

TABLE V. COMPARISON OF PROPOSED MODEL WITH CONVENTIONAL & [12]

	Transistor Count	*Static Power*	*Dynamic Power*	*Total Power*
In[12]	24	1.49E-06	5.774E-06	7.89E-06
Conventional decoder	36	2.298E-06	5.593E-06	7.89E-06
Proposed decoder	24	1.512E-06	5.634E-06	7.89E-06
%age Improvement wrt Conventional	33.33	33.85	-0.7	9.44
%age Improvement wrt In[12]	0	-1.47	2.245	1.6

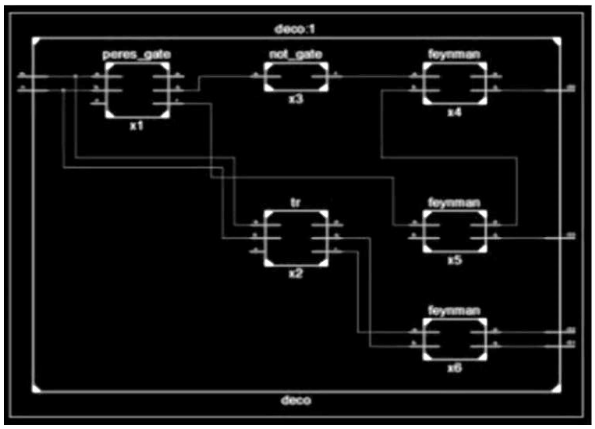


Figure 9. RTL View of 2 ×4 Decoder

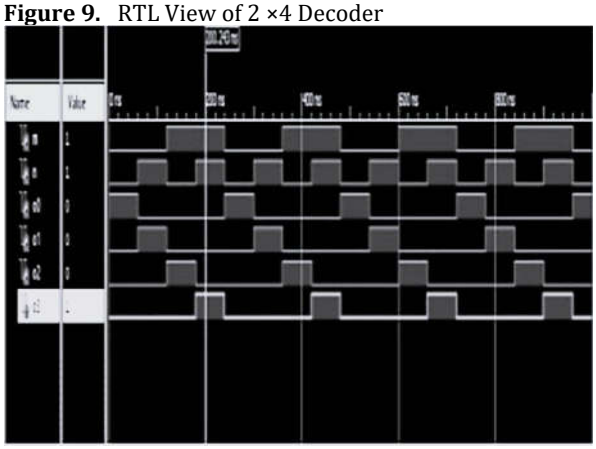


Figure 10. Output Waveform of 2 ×4 Decoder

V. CONCLUSION

The Decoder circuit finds ample applications in low power based design and implementation of the different dominant modules of the qALU that in turn improves the output of the processors with it's utilization in the fields of computerized plans, quantum processing, nanotechnology, DNA registering and so on. The basic issues involved in the testing and planning of the reversible circuits is to advance the various boundaries which result the plan expensive. In this paper, we propose an original plan of a reversible 3-to-8 decoder that acknowledges considerable improvement over existing ones as far as quantum cost, trash yield, consistent data sources, and number of doors. We found that the effectiveness and Supremacy of the methodology with a few hypothetical clarifications it tends to be demonstrated. In any case, further scientist interest might be to propose new doors that can be utilized to supplant existing ones in higher layered decoders, bringing about diminishing of quantum cost and different boundaries.

ACKNOWLEDGMENT

The author is thankful to Late Prof (Dr.) Arun Gupta (Ex-Chairman, MIER Group), Dr. Renu Gupta (Chairperson, MIER Group), Prof. (Dr.) Ankur Gupta, Director, Model Institute of Engineering & Technology (Autonomous), Jammu, Prof. (Dr.) Ashok Kumar, Dean Academic Affairs & HoD, ECE, Prof. S K Sharma, Prof. G S Sambyal as well as faculties & staff of ECE Department for their motivation, kind cooperation, and suggestions.

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