12T MEMORY CELL FOR AEROSPACE APPLICATIONS IN NANOSCALE CMOS TECHNOLOGY

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Abstract—

The size of semiconductors and the distances between them are rapidly shrinking as technology advances. As a result, SRAM cells used in aerospace applications become more susceptible to soft-error when the fundamental charge of the fragile nodes decreases. Single-event upsets (SEUs)may cause data inversion if a radiation particle hits a sensitive node in a typical 6T SRAM cell.To lessen the impact of SEUs, this paper proposes a Soft-Error-Aware Read-Stability-EnhancedLow-Power12T (SARP12T) SRAM cell. SARP12T's performance is evaluated in relation to those of other recently released soft-error-aware SRAM cells such as QUCCE12T, QUATRO12T,RHD12T, RHPD12T, and RSP14T. Even if the values of the sensitive nodes in SARP12T areflipped due to a radiation attack, the data may be recoverable. SARP12T is resilient to storagenode-pair-initiated single-event multi-node upsets (SEMNUs). The '0' storing memory nodes in the proposed cell are easily accessible through the bit line during read operation and are highly resistant to interruptions. SARP12T is also the most efficient method of holding in terms of energy consumption. SARP12T out performs competing cells in terms of write performance, and its write latency is much lower. The suggested cell achieves all of these advantages with just a little increase in read latency and read/write energy.

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I.   Introduction

Thestrongionizingeffectofradiationnearnuclearreactor sandinspacehasthepotentialtoimpairor   destroy electrical infrastructure. Ionizing radiation has been linked to circuit failures, notablyin data storage devices. The scientific community uses the term "single   event   upset"   (SEU) todescribetheoccurrenceofseveralionizingeffectsofra diationatonce[1,2].Ontheonehand,theidea   that this radiation doesn't have any effect on long-term memory seems conceivable. Whenmany events occur at once, it may cause an electronic equipment to malfunction,   a phenomenonknownasthe"singleeventmulti-upseteffect"(SEMU)[22].Resetting[7]theelectricalcycle withsoftware that employs state machines to recognize prior states might reduce radiation risks.Spending a little amount on space-related

applications won't alter this fact [4]. Bit flipping inionizing CMOS [16] memory is the source of a soft mistake [17]. This impact is due to theexpansion of pores in the oxide layer. This strategy makes data storage very sluggish to access.When evaluating SRAM memory in the presence of ionizing radiation, it may be helpful to use awrite cycle of different time and complexity to better display the findings. Every new generationof technology results in smaller and more powerful integrated circuit machines. The goal of thistechnique, which makes use of integrated circuits, is   to   increase   output   by   packing   as manycomponentsintoagivenspaceas   feasible. AsMoore'slawhasbeenroughlyfollowed,thesizeoftransi stors,thefundamentalbuildingblocksofmemorycells,ha srisen.So,itstandstoreasonthatcell   density   will gradually reduce with each succeeding generation [1]. Due to the small size ofthe transistors used in contemporary   technology,   each   individual   cell

constitutes a nanoscalesystem; this is how SRAM-compatible metal-oxide-semiconductor (CMOS) memory is created.As a result, SRAM chips are able to function at steadily decreasing voltages. The InternationalTechnologicalStrategyforSemiconductors (ITRS)predictedthatthistrendwouldreverse,buttheopposite has already occurred. The scaling limitation on the threshold voltage of the transistorkepttheleakagecurrenttoanacceptablelevel[2].Thesestaticrandomaccessmemories(SRAMs)areessentialtotheoperationofmanycontemporaryelectronicdevices.Thisneedhasbeenmetinlargepartthroughtheallocationofdedicatedspace.Costsareanticipatedtoincreaseasthepredicted number of patients exceeds 90% [3. The technicians are trying to fit as many SRAMcellsastheycanintoeachpart.Becauseitresultsincellsthataresmaller insize,thisprocedureiscrucial for improving the technology. SRAMs have transistors that are normally as small and ashigh up in the architecture as is practicable. Additionally, the voltage is maintained low to easestrainontheelectricalsystem.However,thereducedpowerusagewasonlypartiallyimplementedin

practice. With the development of new technologies, SRAM devices have become smaller anduse less power; nonetheless, the design still has to overcome two significant obstacles, namely,cellstabilityandtransienteventradiation.Thisstudyfocusesonthelatterphenomenon.However,therearealsoinquiriesintoSRAMdependabilityconcerns.Intermsofregionalradiation,SRAMsare crucial. They might be badly damaged by single-event upsets (SEUs), which are triggered bya single particle of energy. These failures are categorized as soft errors (SE) since they do notpermanently harm the circuit. When massive particles collide, they release electron-hole pairs(SEUs),whicharegatheredinasensitiveregionandutilizedtocontrolthecircuit'spowersupply.A node in an SRAM array may check the status of a cell and change the data stored in it if thereisenoughnoise.Thereisnotruthtotheseclaimsatall.OneormoreSRAMcellsmighthavetheirdata corrupted by a passing particle.

I. PROPOSEDMETHOD

This novel radiation-hardened-by-design (RHBD)12T storage facility features aneasily implementable layout-topology and also takes into consideration the physicalmechanism of upset in soft faults. The validation results show that the proposed 12Tcell can provide significant radiation resistance. The predicted 12T cell requires

moreroom,energy,andtimetoreadandwritethan a13Tcell.The986.2mVmarginofstaticnoise in the hold is more than what a 13T cell can achieve. The error-correctingcapabilitiesoftherecommended12Tcellmakeitmoretrustworthy.Thesedays,CMOStechnology is ubiquitous in the electronics sector. The aircraft industry is another thatbenefitsgreatlyfrom CMOStechnology.Memoriesaretheprimary datastoragemechanisminmanyaeronauticalapplications.CMOStechnologyisusedintheproduction of SRAM cells, a kind of memory. The main problem with long-termmemory is single-eventdisruptions (SEUs), which are brought on by particles ofradiation. Rising urbanization is directly responsible for the SEUs. As CMOS processtechnology has advanced, both the critical charge and supply voltage have decreased.A approach free of these SEUs is needed for use in aircraft systems. Where exactly dothey exist in the very radioactive void between the stars? Methods that are radiation-hardenedby design (RHBD)thatare resistanttosofterrorsarecurrentlybeingresearched.Theprimarycontributionofthisstudyisaproposalforalow-profile,high-reliabilityRHBDmemorycell.

"Adiabaticlogic"referstolow-powerelectricalcircuitsthatmaybeemployedineitherdirection. During the adiabatic phase, there is no change in the total quantity of heat orenergy in thesystem,thusthename.Energy dissipationisgreatlyimprovedbydecreasingcircuitsizeandincreasingcircuitfineness,whichhasbeenamajormotivationforstudyingadiabaticcircuits.

A. SCRLNAND

Understanding the bigpicture behind this group of genes may require dissecting the SCRL NAND completeloopshowninFigure1.

ThisNDusestrapezoidalclocks(Kin1 and/Kin1)topowerthetopandbottomtracks,rather than the more conventional Vdd and Gne 1. There has been no change to thissection. With the exception of P 1, which is connected to Gnd, and /P 1, which isconnected to Vdd, all components are linked to Vdd/2 in the first position, renderingthe switch gate superfluous. The transmission gate is turned on once P 1 and P 1 areconfigured.Firststeps.VddandGndarethencreatedfromthe/first1and/first1Vdd/2nodes.   At

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this stage, the NA ND of both a and b go through the same non-adiabaticdoorcalculation.Oncetheoutputisbeingutilizedbythesubsequentgate,thetransmitting gate may be gradually disabled. The input may be adjusted and the nextphase initiated once the sum of phases 0 and 1 reaches Vdd/2 again. Since a deviationfrom Vdd/2 would violate the first criterion, a resistor must be disabled and the railsresettothisvalue.
P-MOS'sfunctionwhencoupledwithBinputisunclear.Pleasereviewthecircumstancesbehind thedisappearance ofthe transistor.Timesoftheeleventhday.
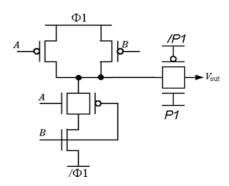

Figure1 :SCRLNAND

B. 2LAL

Frank's[2] Another significant class of adiabatic circuits is the 2LAL family. Thisseries, like SCRL, has complete plumbing all the way to the gate. Figure 2(a) depictsthe fundamental components of 2LAL, a pair of transmission gates used to representthesignalsAandA.BecauseofitssimplicityandindependencefromCMOS,2LALiswellsuitedforimplementationincutting-edge devices.

Two transmission gates make up the 2LAL basic buffer feature, seen in Figure 2(b).Eachtrapezoidalclock'szero pointonthefourthcyclehappensoneandaquartertimeslater than the other. Both vertices start out with a value of 0 at the beginning. If theinputis1,the state willchangefrom0 to1overtime.Whenwegoonto"phase 1,"
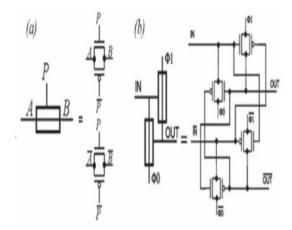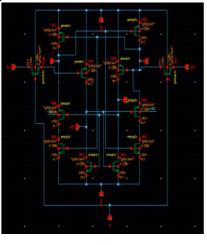

Figure 2: 2LALBasicGate(a) andBuffer(b)

Whentheinput is1,theoutputand inputarebothsetto 1,andthetransistorisdisabledto save power. Finally, switch the input back to 0 and keep cycling between 1 and 0.Thepipelineisreadytoacceptanewinputaftertheoutputpassesthroughthenextgateand reverts to 0. 2LAL can build inverters quickly since rails may cross from one porttoanother.

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II. RESULT
A. *Proposed schematic*
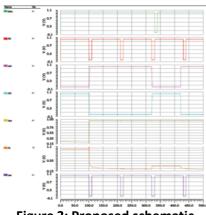

Figure 3: Proposed schematic

Figure4 : proposed schematic simulation result

A. DELAY

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Parsing                 0.01 seconds
Setup                   0.05 seconds
DC operating point      0.07 seconds
Transient Analysis      0.03 seconds
Overhead                0.91 seconds
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Total                   1.07 seconds
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A. POWER

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Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
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CONCLUSION

Theunique12TRHBDmemorycelldevelopedher elessenstheeffectofsoftmistakesin standard 65 nm CMOS technology. The proposed memory cell is an advancementover prior designs in a number of respects; most importantly, it is more resistant todisturbances that damage several nodes. 1000 MC simulations further corroborate theprocess's SEU robustness by demonstrating that no changes to the process affect theSEU's stability. Some high-speed applications may be slowed down by the proposed12T memory cell because of its slower read access time compared to existing memorytechnologies.Memorysize,robustness, andreliabilitymaybeoffargreaterimportancein mission-critical aircraft applications. In light of this, the RHBD 12T memory cellreported in this paper is, from the standpoint of a critical application designer, anexcellentdesignforradiationresistancewhen comparedtootherstate-of-the-arthardened memory cells. Increasing the paper's speed while decreasing its footprint is acommonmethodofimprovement. OneofthetrickiestNano-scaledependabilityissuestosolveistheBTI,which modifiesthe transistor's Vth value. Changing the Vth of SRAM transistors degrades the qualityofSNMs.Inthisstudy,wedescribeasensor thatcandetectBTIdeteriorationinSRAMcells with high accuracy, allowing for the monitoring of this process over time. Thepeak Ivdd/Ignd of the SRAM block during a write operation may be used as a proxyfortheNBTI/PBTIagingofindividualSRAMce lls.TheCCVSmeasuresandconvertsthis current to voltage. The fundamental frequency of the VCO's oscillation is set bythemaximumvalueofthisvoltage.Thefrequen cyoftheoscillationsmaybecomparedto that of newly created cells to observe the impact of BTI. Reading the appropriateiteminthe SRAMmayrevealthe roworcell's BTIcondition.

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