FPGA Implementation of Area and Power Optimized and High Speed Seizure Detection System using ELM Classification Method

K.R. Radhakrishnan[1*], M. Amalasweena[2], T. Kesavamurthy[3]

Abstract

In order to diagnose brain abnormalities, electroencephalography (EEG) signals are employed. The aberrant electrical activation in the nervous system of human which is recorded by these EEG signals defines the epileptic seizures. Seizure sufferers might die suddenly if these epileptic seizures occur at an inappropriate time. It is possible to identify and anticipate epileptic seizures by studying these EEG data signals however it is a difficult process to analyze reliable prediction. As a result, more precise epileptic seizure detection is possible recognition to hardware and real-time FPGA implementation. Brain rhythms in the delta (0–4Hz) and theta (>4Hz) bands were studied separately in this approach, which used the band pass fixed impulse responses. In the application of digital signals processing , multiplication is more priority one its restricted in number and have fixed position on FPGA, which may cause routing delays and lower bit width of optimized soft IP core. This paper presents that soft multiplier IP core of Accurate and Approximate Multipliers instead of MCM multiplication was used in every band of FIR filters and Feature extraction approach and ELM Classification in this suggested study for the reduction of area, power and delay of the EEG data and for classifying normal or epileptic signals. Finally, this suggested study compared all parameters on the basis of delay, power and area, and was developed in Verilog HDL and generated in Xilinx Virtex-5 FPGA.

KeyWords: Approximate Computing, Multipliers, FPGA, Electroencephalography (EEG), ELM, Epileptic Seizure, Linear prediction.

DOI Number: 10.14704/NQ.2022.20.12.NQ77135 **NeuroQuantology 2022; 20(12):1571-1580**

Introduction

Epileptic seizure disorder refers to a pattern of sudden, erratic, and recurrent responses shown by the human brain. Diseases that induce epileptic seizures affect 70 million individuals throughout the globe, putting their lives in danger. Electrodes are placed on the scalp in order to assess electrical activity emanating from the human brain during an EEG. The signal from the EEG exhibits a high degree of similarity to the activity of the brain. Therefore, the signal from an EEG is often employed for the detection and diagnosis of seizures. Optic inspection is a technique that is used by the EEG professionals to detect the epileptic seizure in humans. The detection and prediction processes both take longer with this technique.

Developing a technology that is capable of automated seizure detection is one way to solve this issue. These fits of convulsions are brought on by unavoidable conditions, and they disrupt the normal functioning of the brain. The suggested technique is related to the amplitude and frequency for the EEG signal and is implemented in FPGA; nevertheless, the algorithm's complexity is enormous in regards of the amount of LUT used in the process, which is the most major restriction of this work. This method employs both the wavelet related features extraction methodology and the FIR filtering approach. Support vector machines are used in order to accomplish the task of signal categorization.

Corresponding author: K.R. Radhakrishnan
Address: [1]Assistant Professor, Department of ECE, PSG College of Technology, Coimbatore, India,[2]Assistant Professor, Department of ECE, R.M.D. Engineering College, Kavaraipettai, India, [3]Professor, Department of ECE, PSG College of Technology,

Coimbatore, India
E-mail: krr.ece@psgtech.ac.in, asm.ece@rmd.ac.in, tkm.ece@psgtech.ac.in

The suggested system will be implemented with the help of the hardware description language Verilog. The gate count, the frequency, the power, and the memory buffer are obtained for the deliberation in the analysis purpose of the performance of the given algorithm [1].

In recent years, there have been a few trials conducted for the purpose of seizure detection with the assistance of two distinct methods. The predictable EEG data is used in the first mechanism, which examines changes in brain activity (spikes, for example) to make this determination. The second process is based on determining whether or not a seizure-free state may be reached by investigating the non-linear evolution of the EEG data according to dominant rule. There have also been a few reported ways that use artificial neural networks that are based on the wavelet transform [2]. This method generates very accurate segment classifications via the use of the artificial neural networks, which is related to extraction of features from number of the different realms.

The wavelet threshold approach is used in order to eradicate the artifacts present in the EEG data. Techniques from the field of information theory are used in order to extract nonlinear characteristics as well as features from the time-frequency domain. In order to identify the most useful characteristics for the classifier, principal component analysis is used. The Support Vector Machine (SVM) Classifier is utilized for carrying out the task of categorizing characteristics.

EEG signals were analyzed utilizing a wavelet technique and also identification is carried out with a SVM classifier. The vast majority of the explorations on seizure identification use an algorithmic technique, rather than one that is dependent on hardware. The algorithms for seizure detection in real time are going to be implemented in FPGA hardware as part of this development [3].

However, the majority of modern precise and approximate multiplier designs exclusively include ASIC related devices. Because of built-in framework dissimilarities betwixt FPGAs as well as ASICs, direct synthesis for these ASIC related multiplier designs for the FPGA related systems results on minimal or no performance increases. To further demonstrate the importance of creating FPGA related approximation components, we give succeeding motivating case study contrasting the performance of ASIC related also FPGA related executions of state of art approximate multipliers which initially created using FPGA Systems.

To create the method suggested in this work for detecting epileptic seizures utilizing approximate signed and unsigned multipliers filtered by FIR. Section II describes the LUT 6 based Approximate Signed and Unsigned Multiplier with FPGA. Section III describes the FIR Filter design using Approximate Signed and Unsigned Multiplier. Section IV describes the proposed approach of Chronic Seizure Detections utilizing the ELM Classifier. Results and Implementation for the suggested signed and unsigned approximation multiplier on FPGA are detailed shown in Section V and Section VI terminates the investigation [5].

Proposed LUT 6 SLICE Structure of Approximate Unsigned & Signed multiplier Architecture

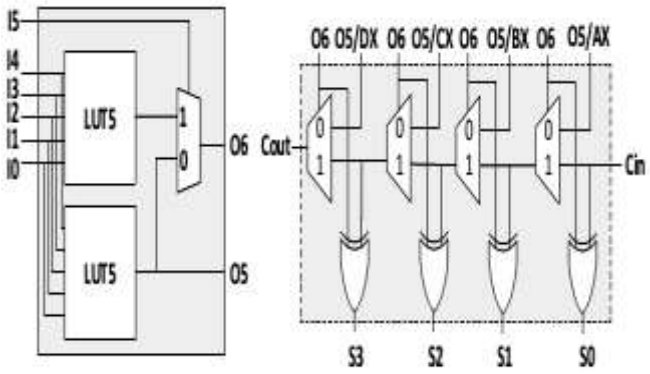

Fig. 1. LUT 6 Architecture using two LUT5 combinational logic with Carry Chain Architecture

Xilinx and Intel's FPGAs, which are among the most advanced on the market use, input-6 LUTs for creating sequential and combinational circuit. All of the designs presented in this book were implemented using Xilinx FPGAs, which we developed specifically for this purpose. Although our approach is general, it may be executed on FPGAs via distinct suppliers, like Intel, that employs factorable carry chains and input-6 LUTs in addition to ours. Four input-6 LUTs (often considered as LUT6 2) are included on customizable logic blocks (CLB) for the Xilinx's 7-series FPGA's [6]. There are also 8 flip-flops to register a singular 4-bit length carry chain and the outputs of LUT in each slice of the CLB.

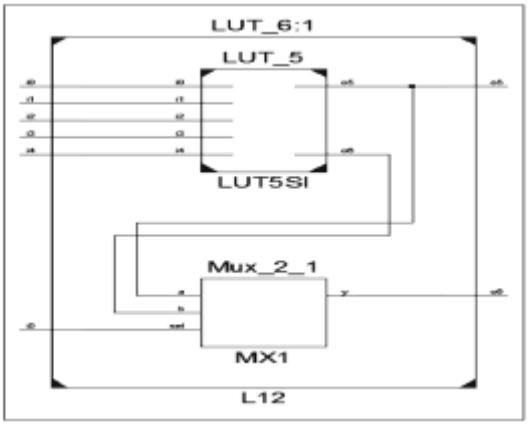

Fig. 2. Proposed LUT 6 Architecture using One LUT5 Combinational Logic and Multiplexer's

In Fig.1, it is shown that the LUT6 structure would be utilized to build either one singular 6-bit combinational process that use output O6 bit or dual 5-bit LUT 5 combinational processes, which are used in the existing method and will require more logic size and power consumptions. Thus the proposed method will re-modify the LUT6 architecture using one 5-bit combinational function with one multiplexer, which will require significantly less logic size and also power utilization when collated with the existing method, and architecture for Proposed LUT6 will shown in Fig.2. A LUT6 2 with the INIT amount of 0000000000000002 (hexadecimal) for example, specifies that it will create outputs O6 is 0 and O5 is 1 when given the input pattern 100001. The executions of combinational processes are not the only thing that is done [7].

$$Si = Pi \oplus ci. \quad (1)$$

$$Ci+1 = Gi + Pi.Ci. \quad (2)$$

Equations 1 and 2 define the carry-look ahead adder, which is implemented by the carry chain, which uses the carry generating signal (O5) and also carry propagating signal (O6). The extraneous bypass signals named as AX – DX may also supply the carry generating signals to the carry chain.

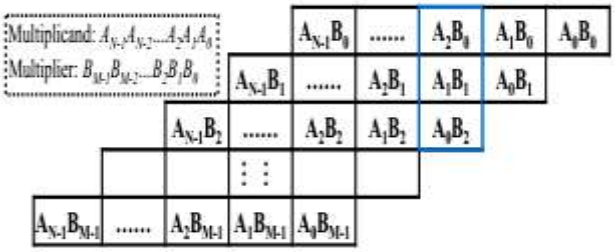

Fig. 3. Design of N x M basic signed and unsigned multiplier partial product generation

When comparing the accurate product of signed multiplication to unsigned multiplication, all partial products must be appropriately sign-extended. There is no longer a need to calculate and transfer sign extended bit since the edification of sign is included with produced partial product. A (N bits) and B (M bits) are multiplied using the basic technique laid out in Fig. 3, that is the basis of the proposed execution of an accurate multiplier. With the 6-input LUTs, we've used the AND process betwixt each bits of both the multiplier also multiplicand for calculating necessary partial products. However, in order to make the most of LUTs, given automatic system combines each second partial product. All of the four groups have a second partial product that has been displaced 1 bit to left side in reference to first partial product [8]. It is also faster and more efficient to compute and combine the partial products of each group at the same time. Partial product terms A0B0 and AN1B1, for example, cannot be coupled with another partial product term in the first group, despite the fact that there are two partial product terms in that group. It is also not possible to group greater than a pair of partial products in a single group due of the restricted no. of input or output pins accessible on LUT's in modern FPGAs. It is impossible to create and add partial products A2B0, A1B1, and A0B2 in a single step, as shown in Figure 3. There are two or more stages required to complete these tasks. Our proposed technique distributes the input-6 LUTs also with accompanying carry chain for every set of partial product in this stage, which is shown in Fig. 6 by computational modules Type-A with Type-B. The term "block" refers to an input-6 LUT also an accompanying adder also with carry chain that may be classified as neither Type-A nor Type-B. (CC) [9].

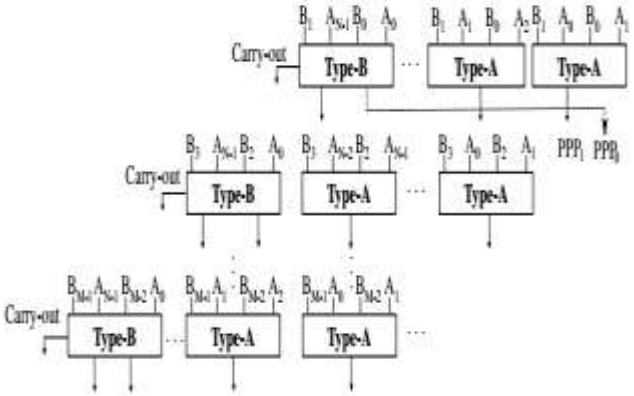

Fig. 4. Partial Products (PPs) generation for the N x M Proposed unsigned approximate

multiplier

LUT of block Type-A is seen in Fig. 5(a), which depicts its operation. O5 and O6 are the output signals that are sent to the related carry chain like carry generating (Gi) also carry propagating (Pi) signals in corresponding carry chain. The O5 function is used in the LUT setup of module Type-B, as illustrated at Fig. 5(b), to calculate the least relevant partial product value for each rows of a block. For such carry chain component that corresponds to Type-B, a constant '0' is used as a generating signal, and these signals are given mostly by extraneous bypass signal (AX–DX), like previously detailed in Fig. 1 and Fig. 2.

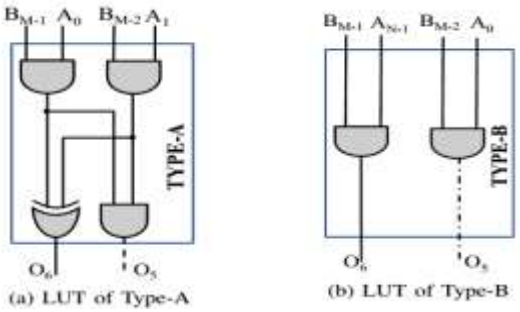

Fig. 5. LUT Configuration for accurate unsigned approximate multiplier

In order to reduce PPPs in each group, we use compressors with a ratio of 3:1 (Full Adder) and 2:1 (Half Adder) in our solution. PPPs reduction might result in the creation of additional partial sums, which are then gathered and run through the 3:1 and 2:1 compressors once again. This procedure is continued until the desired result is achieved. As seen in Fig. 6, the 8x8 multiplication architectural process generates 8 PPPs, which is equivalent to a 16x16 multiplier generating PPPs Fig. 7 illustrates the process of combining and reducing these PPPs in order to calculate the final result [10].

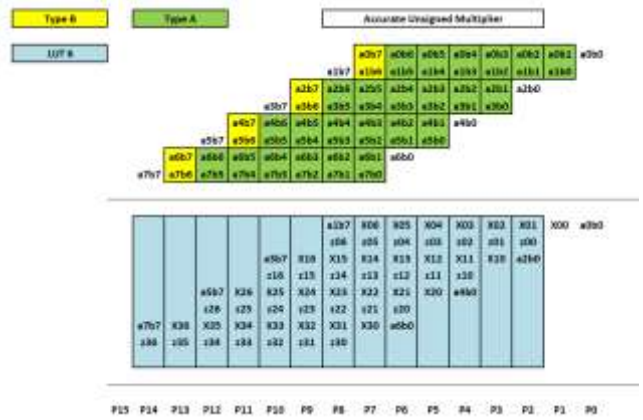

Fig. 6. 8x8 Approximate Unsigned Multiplication architecture using TYPE A, TYPE B and LUT 6.

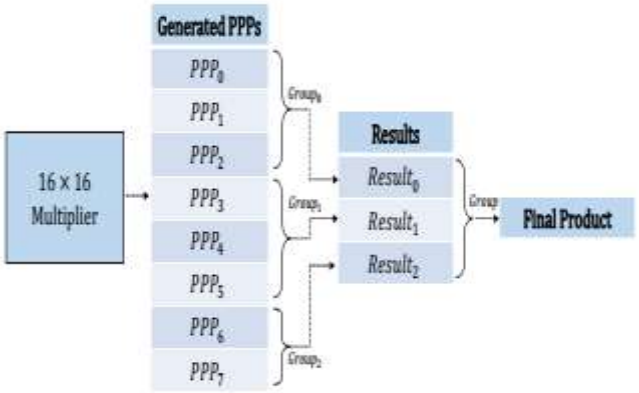

Fig. 7. PPPs grouping for computation of final product for 16×16 multiplier

We show our innovative design for the accurate signed multiplier, which is related to the suggested approximate signed multiplier of Baugh Wooley's method for multiplication and the proposed approximation signed multiplier. Our algorithm creates just M/2 signed PPPs for a signed multiplier with the N x M coefficients. This characteristic of our suggested solution is equivalent with commonly deployed radix-4 Booth's technique for multiplication that minimizes the overall partial products created by half.

Moreover, the method for Baugh Wooley's removes this requirement of additional sign extended bits that makes it possible to construct the multiplier in a more resource-efficient manner. Illustration of the method of Baugh Wooley's as a graphical form is shown in Fig. 8. A complement is formed by combining the row of final partial product with more important terms in other all previous partial product rows, as shown in the example. The creation of these supplemented words necessitates a modification to our proposed design flow, which

includes the addition of three additional LUT configurations [11].

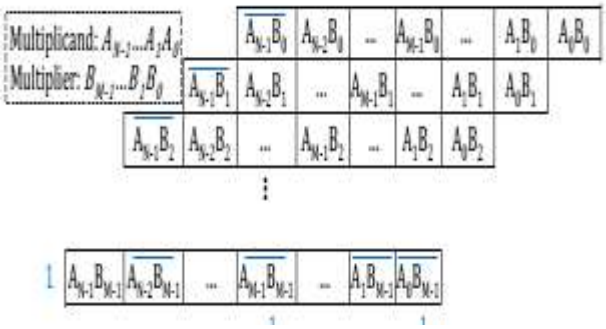

Fig. 8. The design for Baugh-Wooley's N x M signed Multiplier

Fig. 9 shows the new LUT configurations that have been added. This stage in our suggested technique for the N x M signed multiplier is shown in Fig. 17 by the LUTs and Carry Chain Assignment step, which is based on these configurations. In order to calculate the final result, we use the 'Re-arrangement with depletion of the PPPs' phase of the proposed technique after creating all signed PPPs and before doing any further processing on them. Furthermore, the 1's at bit positions 2 N1, 2M1, and 2 N+M1, as laid out in Fig. 8, also inserted while the last phase for the reduction of PPPs, which is illustrated in Fig. 10 [12].

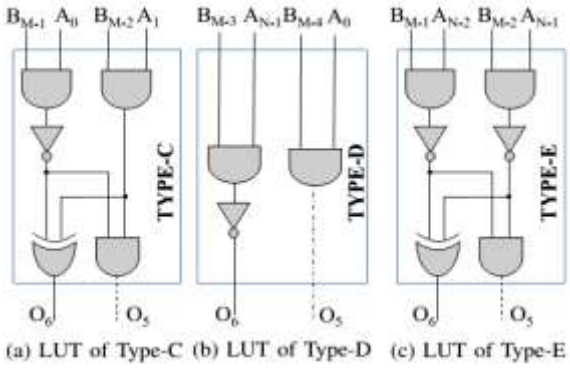

Fig. 9. LUT Configuration for accurate and approximate

Signed multiplier

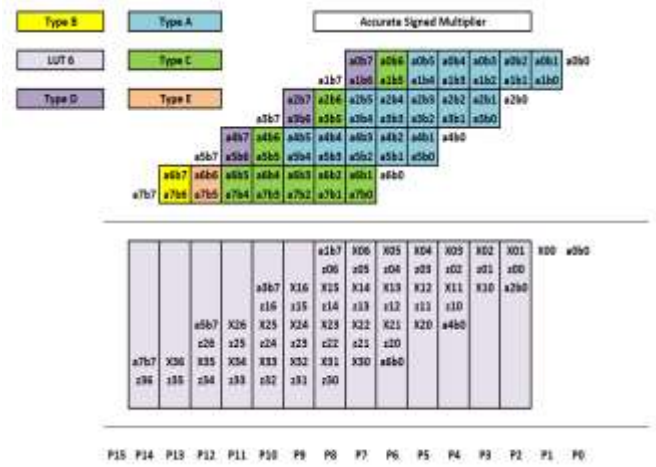

Fig. 10. 8x8 Approximate Signed Multiplication architecture using TYPE A, TYPE B, TYPE C, TYPE D, TYPE E and LUT 6.

Proposed FIR Filter design using Approximate Signed and Unsigned Multiplier

With reference to low and high sampling range, noise reduction and impulse response, cut-off frequency and filtering order, Finite Impulse Response (FIR) often used for assisting DSP applications. A multitude of mathematical operations, including multiplication, subtraction, addition and delayed elements must be needed for decomposing response coefficients for low pass; high pass; band pass along with stop filters. There is no possibility for rounding errors in arithmetic operations of these FIR filters, and they are constitutionally reliable for producing significance outputs also this didn't acquire maximal value at the order of Nth impulse response, which makes it easy to design and configure, and it can be used in applications such as mastering and seismology. It is possible, using this FIR filter technology, to get a coefficient that is appropriate in both the frequency and temporal domains. Since Nth-order multiplication, addition, and subtraction are used in the FIR filter, its biggest drawback is its enormous surface area and high power consumption [13] & [14]. A pipelined method of significant computation results is produced in the High Performance Digital Signal Processing method by using MCM (Multiple Constant Multiplication) at each and every arithmetic operation with this is similar to design of FIR Filter, where the transpose form of MCM based FIR is acceptable for the largest order filter execution along with finite coefficients, however it will consume largest area also power. An accurate and approximate multiplier was employed in the

FIR Filter design instead of MCM multiplication for this substantial area and power reduction, as seen in the FIR Filter architecture in Fig. 11.

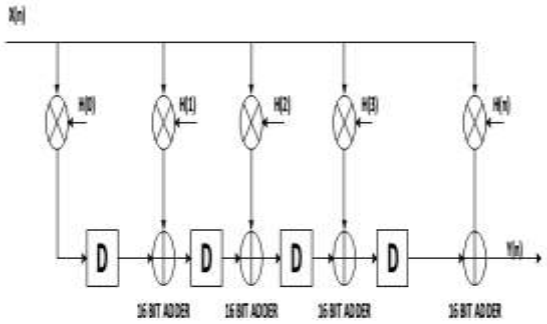

Fig. 11. FIR Filter Design using Approximate Multipliers

Proposed Approach of Epileptic Seizure Detections using ELM Classifier

The outline of the suggested strategy that was used in this work is shown in Fig. 12. A band pass filter can be utilized at the input EEG signals in order to remove any undesired factors that may be present in the signal. The EEG signal is divided into the following five EEG sub bands by using a band pass filter: Delta (frequency range: 0 to 4 Hertz), Theta (frequency range: 4 to 8 Hertz), alpha (frequency range: 8 to 12 Hertz), beta (frequency range: 13 to 30 Hertz) and Gamma (>30 Hertz). Xilinx System block set was used throughout the design process for the band pass filter. In order to further model the segmented band signal, the linear prediction theory is used. This theory is what is used to estimate the random amount based on particular data that is accessible [15].

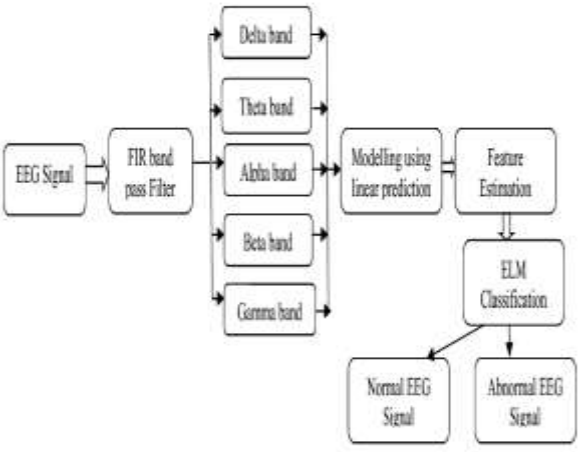

Fig. 12. Block Diagram of Proposed Epileptic Seizure Detection System

The statistical features from every sub band were extracted initially in order to construct a feature vector. ELM classifier is applied at the signal in question in order to determine whether or not a seizure is taking place. The Xilinx System block set is used in the development for the both, algorithm for ELM classifier and the process of feature extraction. The use of a band pass FIR filter is what is required to acquire the individual EEG sub band signals. The FIR filter has many benefits, including linear phase analysis, analysis of scale space also high stability. Gamma, Beta, Alpha, Theta and Delta are the names for the sub bands that are included inside the basic EEG signal. The EEG dataset that was utilized in this investigation has a sampling frequency of 173.61 hertz.

The sampling theorem of Nyquist states that greatest frequency that may be conveniently sampled is equal to half of its frequency of sampling (i.e. 86.81 Hertz). The pass band cut of frequency in a band pass filter is determined by the relative frequencies of the various sub bands. The FDA tool this is included with the Xilinx Device block set, is used to the designing process of the filter coefficient for the necessary filter and comparisons table shown in Table 1, comparisons analysis chart shown in Fig. 13.

Results and Implementations

In this study, the performance of the system is evaluated based on both 100 EEG signals derived from seizures and 100 EEG signals derived from normal brain activity.

Each individual EEG signal is captured at a frequency of 173.6 Hz. The FIR band pass filter is utilized for deconstructing given EEG signals as its component sub bands of Gamma, Beta, Alpha, Theta and Delta. Band pass filter is a Features Extracting Block, FIR (Finite Impulse Response) as well as Classifier ELM's FIR. Findings of the ModelSim simulation for the detection of epileptic seizure are displayed in figures 14 (normal EEG Signal) and 15 respectively (Abnormal EEG Signal). The device consumption summary for the detection of epileptic seizure architecture is laid out in Fig. 16, delay report is displayed at Fig. 17, the schematic for RTL is displayed at Fig. 18 also the power report displayed at the Fig. 19. These implementation results are obtained from Xilinx ISE Design Suite 14.5 Software.

Table I : Comparisons Of Epileptic Seizure Detection Using High Performance Accurate And Approximate Multipliers

Parameters	Epileptic Seizure Detection using Approximate Unsigned Multiplier	Epileptic Seizure Detection using Approximate Signed Multiplier
Number of Slice Registers	2430	2412
Number of Slice LUTs	5791	6102
Number of Occupied Slices	1859	1967
Number of bonded IOBs	16	16
Delay (ns)	23.504	23.556
Power (W)	0.637	0.646

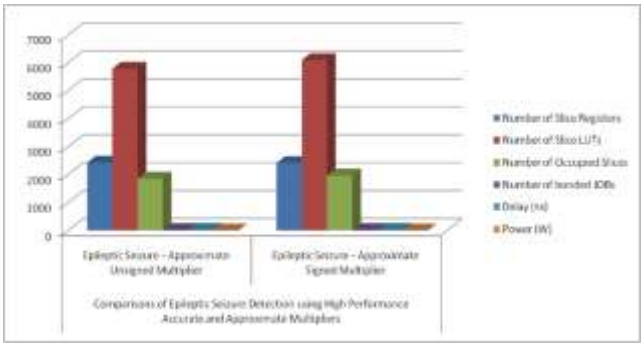

Fig. 13. Comparisons Analysis Chart of Epileptic Seizure Detection using High performance Accurate and Approximate Multipliers

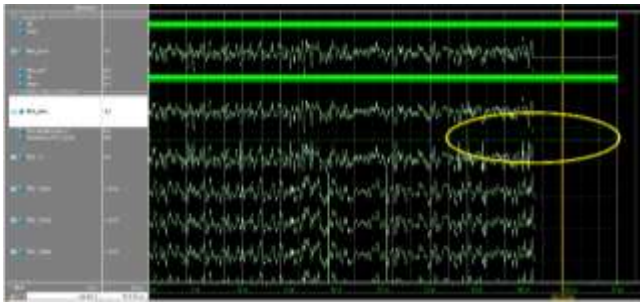

Fig. 14. Simulation output of Normal Seizure Predictions using highly efficient Accurate and Approximate Multipliers

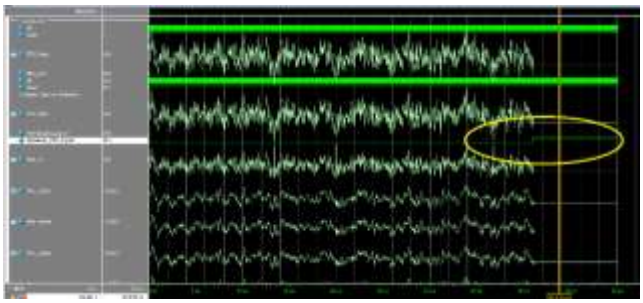

Fig. 15. Simulation output of Abnormal Seizure Predictions using highly efficient Accurate and Approximate Multipliers

Fig. 16. Design summary of Seizure Predictions using Approximate Unsigned Multiplier

Fig. 17. Delay report of seizure prediction using unsigned Approximate Multiplier

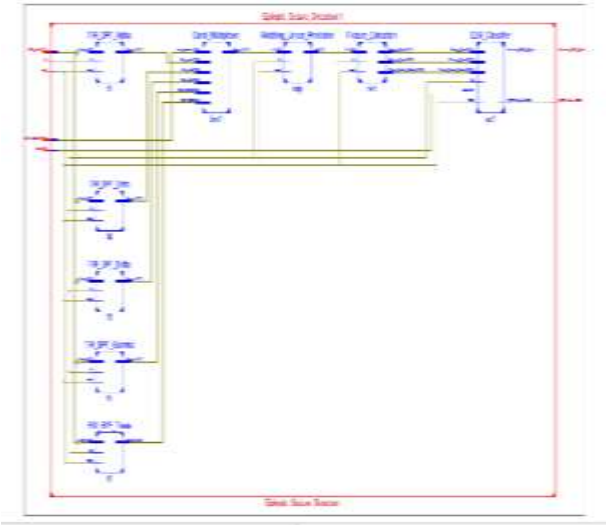

Fig. 18. RTL Schematic of Seizure prediction using Unsigned Approximate Multiplier

Fig. 19. Power report of Seizure prediction using Unsigned Approximate Multiplier

Conclusion

In a recent application, the mathematical operations of multiplications were used. These multipliers may cause appended routing latencies also could be ineffective with multiplications for lower bit width, both of which may result in increased power consumption. The EEG data was analyzed to identify epileptic seizures, and the ELM algorithm was used to classify them. When analyzing EEG data, a band pass filter is used to remove unwanted noise. ELM Classifier with Accurate and Approximate Multiplier is used to detect epileptic seizures. These architectures take advantage of FPGA's features for the fundamental architecture such as fast carry chains and LUT (look-up table) framework, to decrease the total latency and also multiplier's resource usage. This is accomplished through the development of generic soft-core multiplier structures that are lower latency, area optimized and accurate also approximate ones. To construct the Accurate and Approximate Signed and Unsigned Multiplier for 8-bit configuration utilizing the technique suggested by this study, and to re-modified the LUT6 architecture by employing a single LUT5 with multiplexers rather than a dual LUT5 with multiplexers for the reduction of the number of multiplexers required. At the conclusion of the procedure, this work was developed in Verilog HDL and synthesized in Xilinx software. All of the characteristics, including area, delay, and power, were compared with one another.

References

"EEG Signal Processing", SaeidSanei and J.A. Chambers Centre of Digital Signal Processing Cardiff University, UK

D. Selvathi, Henry Selvaraj, "FPGA Implementation for Epileptic Seizure Detection using Amplitude and Frequency Analysis of EEG Signals"' , 25th International Conference on Systems Engineering, ISBN: 978-1-5386-0610-0,2017

SreethuRaj ,Anuja George, "FPGA Implementation of EEG Feature Extraction and Seizure Detection" , International Journal of Innovative Research in Science, Engineering and Technology Vol. 5, Issue 9, September 2016 ,pp 16347-16352

C. JohnMoses,1 D. Selvathi,2 and V.M. Anne Sophia1, "VLSI Architectures for Image Interpolation: A Survey" ,Hindawi Publishing Corporation ,VLSI Design ,Volume 2014, Article ID 872501, 10 pages

Iasemidis, L. D., 'Epileptic seizure prediction and control', IEEE Trans. Biomed. Engng., 50, 2003, 549–558.

Annegers, J. F., 'The epidemiology of epilepsy', in The Treatment of Epilepsy, Ed. E. Wyllie, Lea and Febiger, Philadelphia, Pennsylvania: 1993, pp. 157–164.

Engel, Jr, J. and Pedley, T. A., Epilepsy: A Comprehensive Textbook, Lippinottc-Ravon, Philadelphias,Pennsylvania, 1997.

H. Adeli, Z. Zhou, and N. Dadmehr, "Analysis of EEG records in anepileptic patient using wavelet transform," J. Neurosci. Meth., vol. 123,no. 1, pp. 69–87, 2003.

N. Brunie, F. de Dinechin, M. Istoan, G. Sergent, K. Illyes and B. Popa, "Arithmetic core generation using bit heaps," 2013 23rd International Conference on Field programmable Logic and Applications, Porto, 2013, pp. 1-8.

J. Beuchat and J. Muller, "Automatic Generation of Modular Multipliers for FPGA Applications," in IEEE Transactions on Computers, vol. 57, no. 12, pp. 1600-1613, Dec. 2008.

Ahmet Kakacak, Aydin Emre Guzel, Ozan Cihangir, SezerGren, and H. FatihUgurdag, "Fast Multiplier Generator for FPGAs with LUT based Partial Product Generation and Column/row Compression," in Integr. VLSI J. 57, C 2017, 147-157.

M. Kumm, J. Kappauf, M. Istoan and P. Zipf, "Resource Optimal Design of Large Multipliers for FPGAs," 2017 IEEE 24th Symposium on Computer Arithmetic (ARITH), London, 2017, pp. 131-138.

E. G. Walters, "Array Multipliers for High Throughput in Xilinx FPGAs with 6-Input LUTs" in Computers, vol. 5, no. 4, 2016.

M. Kumm, S. Abbas and P. Zipf, "An Efficient Softcore Multiplier Architecture for Xilinx FPGAs," 2015 IEEE 22nd Symposium on Computer Arithmetic, Lyon, 2015, pp. 18-25.

H. Parandeh-Afshar and P. Ienne, "Measuring and Reducing the Performance Gap between Embedded and Soft Multipliers on FPGAs," 2011 21st International Conference on Field Programmable Logic and Applications, Chania, 2011, pp. 225-231.

S. Ullah et al., "Area-optimized low-latency approximate multipliers for FPGA-based hardware accelerators," in Proc. 55th ACM/ESDA/IEEE Design Autom. Conf. (DAC), San Francisco, CA, USA, 2018, pp. 1–6.

S. Ullah, H. Schmidl, S. S. Sahoo, S. Rehman, and A. Kumar, "Area optimized accurate and approximate softcore signed multiplier architectures," IEEE Trans. Comput., vol. 70, no. 3, pp. 384–392, Mar. 2020, doi: 10.1109/TC.2020.2988404.

Salim Ullah, Semeen Rehman, Muhammad Shafique and Akash Kumar, "High-Performance Accurate and Approximate Multipliers for FPGA-based Hardware Accelerators", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022.

S. Ullah, S. S. Murthy and A. Kumar, "SMApproxlib: Library of FPGA based Approximate Multipliers", in 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC), San Francisco, CA, 2018.

V. K. Chippa, S. T. Chakradhar, K. Roy and A. Raghunathan, "Analysis and characterization of inherent application resilience for approximate computing," 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC), Austin, TX, 2013, pp. 1-9.

A. K. Verma, P. Brisk and P. Ienne, "Variable Latency Speculative Addition: A New Paradigm for Arithmetic Circuit Design," 2008 Design, Automation and Test in Europe, Munich, 2008, pp. 1250-1255.

M. Shafique, W. Ahmad, R. Hafiz and J. Henkel, "A low latency generic accuracy configurable adder," 2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, CA, 2015.

V. Gupta, D. Mohapatra, A. Raghunathan and K. Roy, "Low-Power Digital Signal Processing Using Approximate Adders," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, pp. 124-137, Jan. 2013.

A. B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," DAC Design Automation Conference 2012, San Francisco, CA, 2012, pp. 820-825.

S. Ullah, T. D. A. Nguyen and A. Kumar, "Energy-Efficient Low Latency Signed Multiplier for FPGA-based Hardware Accelerators," in IEEE Embedded Systems Letters, DOI: 10.1109/LES.2020.2995053.

M. Kumm, M. Hardieck, J. Willkomm, P. Zipf and U. Meyer-Baese, "Multiple constant multiplication with ternary adders," in 2013 23rd International Conference on Field programmable Logic and Applications, Porto.

C. Liu, J. Han and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2014, pp. 1-4.

C. Lin and I. Lin, "High accuracy approximate multiplier with error correction," 2013 IEEE 31st International Conference on Computer Design (ICCD), Asheville, NC, 2013, pp. 33-38.

H. Parandeh-Afshar, P. Brisk and P. Ienne, "Exploiting fast carry-chains of FPGAs for designing compressor trees," 2009 International Conference on Field Programmable Logic and Applications, Prague, 2009, pp. 242- 249.

K. Bhardwaj, P. S. Mane and J. Henkel, "Power- and area-efficient Approximate Wallace Tree Multiplier for error-resilient systems," Fifteenth International Symposium on Quality Electronic Design, Santa Clara, CA, 2014, pp. 263-269.

P. Kulkarni, P. Gupta and M. Ercegovac, "Trading Accuracy for Power with an Underdesigned Multiplier Architecture," 2011 24th Internatioal Conference on VLSI Design, Chennai, 2011, pp. 346-351.

S. Hashemi, R. I. Bahar and S. Reda, "DRUM: A Dynamic Range Unbiased Multiplier for approximate applications," 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, 2015, pp. 418-425.

S. Rehman, W. El-Harouni, M. Shafique, A. Kumar, J. Henkel and J. Henkel, "Architectural-space exploration of approximate multipliers," 2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, 2016, pp. 1-8.

J. Mody, R. Lawand, R. Priyanka, S. Sivanantham and K. Sivasankaran, "Study of approximate compressors for multiplication using FPGA," 2015 Online International Conference on Green Engineering and Technologies (IC-GET), Coimbatore, 2015, pp. 1-4.

V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan and K. Roy, "IMPACT: IMPrecise adders for low-power approximate computing," IEEE/ACM International Symposium on Low Power Electronics and Design, Fukuoka, 2011, pp. 409-414.

V. Mrazek, R. Hrbacek, Z. Vasicek and L. Sekanina, "EvoApprox8b: Library of approximate adders and multipliers for circuit design and benchmarking of approximation methods," Design, Automation & Test in

Europe Conference & Exhibition (DATE), 2017, Lausanne, 2017.

C. R. Baugh and B. A. Wooley, "A Two's Complement Parallel Array Multiplication Algorithm," in IEEE Transactions on Computers, vol. C22, no. 12, pp. 1045-1047, Dec. 1973, doi: 10.1109/T-C.1973.223648

I. Kuon and J. Rose, "Measuring the Gap Between FPGAs and ASICs," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 2, pp. 203-215, Feb. 2007.

Garima Chandel, Omar Farooq, Yusuf U Khan, Yash Vardhan Varshney, "Patient Specific Seizure Onset-Offset Latency Detection using Long-term EEG Signals," 2019 International Conference on Electrical, Electronics and Computer Engineering (UPCON), 1-6, 2019.

J Prabin Jose, M.Sundaram, G.Jaffino, "FPGA Implementation of Epileptic Seizure Detection Using ELM Classifier", 2020 Sixth International Conference on Bio Signals, Images, and Instrumentation (ICBSII), 1-5, 2020.