Design of Tunnel FET based Low Power Adder for Biosensor Application

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Abstract-
Based on the concept of band-to-band tunneling, tunnel FETs (TFETs), which have lower leakage current and a sub-threshold slope than MOSFETs, are discovered to be a promising option for extremely low power electronic applications. But it's crucial to examine how these devices perform in analog and digital circuits in comparison to traditional MOSFETs. Since TFETs are currently only used in research, circuit simulators do not include built-in models for these devices, making it impossible to simulate circuits using TFETs. The objective of this work is to use Verilog-A to integrate an analytical model of TFET based on physics into the Cadence build framework, and to use the integrated model to build and simulate digital circuits. In Cadence, a library containing all fundamental TFET-based logic gates is produced. A library is created in Cadence which includes all basic logic gates based on TFET using which full adder circuits are realized. The proposed Tunnel FET based full adder device has recommended ate for first-rate potential as a capable contender for replacing MOSFET in low-energy, high-performance applications such as Tunnel FET based Biosensor for Health-IoT Applications.

Index Terms: TFET, Leakage power, Reliability, Band to Band tunnelling, Full adder
DOI Number: 10.48047/NQ.2022.20.13.NQ88513 Neuroquantology 2022; 20(13): 4214-4219

1-Introduction

In Health care and Monitoring, IoT plays a vital role to diagnosis, monitor, evaluate and notify the patient information as well as it also provides the possibility to connect sensor and other devices to the internet. Few examples on IoT based Health care are: BP monitors, Glucose monitor, Sensor embedded in medical equipment etc. [1] Internet of things (IoTs) have attracted huge attention towards the field of information and communication technology (ICT). This technology plays an important role for providing facilities and services for Healthcare. In term of Healthcare-IoT systems, biosensor is also an essential component which is used for real time monitoring, and early stage detection of a disease. It has also been used for checking the prescribed treatment given for a patient. In many places, poor medication becomes a major problem for patient as well as healthcare providers due to rapid growth in population. It is noticed that about 25% of the ageing population do not follow to their given medication which leads to poor health and an increment in death.

Therefore, a biosensor is needed for healthcare-IoT applications, which can improve the medication among people with the help of connecting through Internet. This biosensor works on bio-molecules conjugation in the nanogap cavity formed by etching the gate dielectric for diagnosis the disease with higher sensitivity and better response time [2].

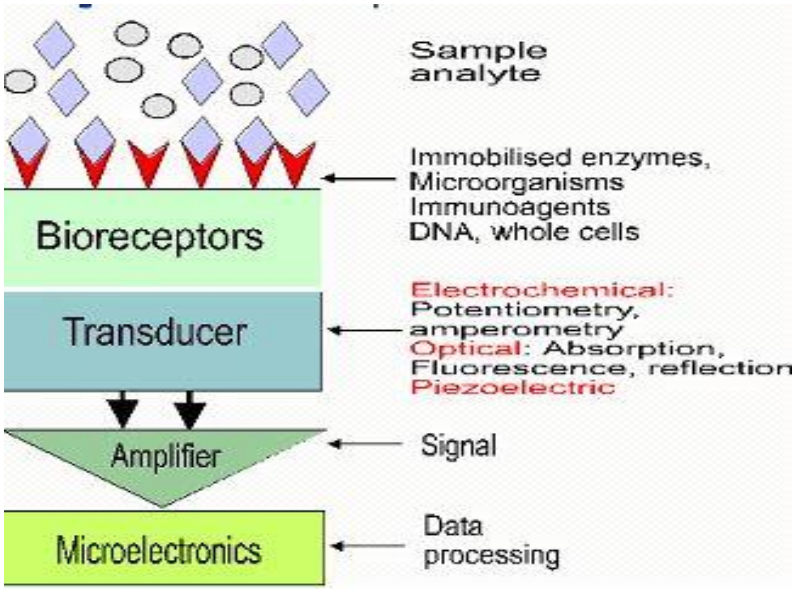

Fig1. Schematic of a biosensor

Basically Tunnel FET is one of the most promising emerging technologies that is posing a challenge to MOSFETs, which are commonly employed in low-power applications. The TFET's functioning is based on the band to band tunneling (BTBT) process, and it has a very low leakage current and a high sub threshold slope.

The sub threshold swing of a MOSFET is

$$s_{s-th} = \ln(10)\frac{kT}{Q}(1+\frac{C_d}{C_{ox}}) \quad (1)$$

Cd=Depletion layer capacitance

Cox=gate-oxide capacitance

$\frac{\mathrm{kT}}{\mathrm{Q}}$= Thermal Voltage

The SS value at ambient temperature (300K) is roughly 60 mV/dec.[3]

The operational frequency of MOSFET-based circuits saturates when device dimensions are reduced because electric field scaling, which requires a reduction in supply voltage, cannot be accomplished. This MOSFET drawback is directly associated with the sub-threshold swing (SS) factor, which at room temperature does not scale beyond 60 mV/dec. Because of its steep slope and low power consumption, the steep-sloped Tunnel FET—whose carrier transport mechanism is electron band-to-band tunneling—has the potential to replace MOSFET [4]. TFET models must be incorporated into circuit simulators and simulations must be run using these models in order to examine the performance of tunnel FET-based circuits. Circuit simulators do not, however, come with built-in TFET models, and the majority of models that have been published are Verilog-A table-based [5, 6]. This paper describes the integration of a TFET model based on physics into Virtuoso, the simulation of a TFET-based complete adder circuit, and the use of Verilog-A in the Analog Design Environment of Cadence design framework.

2-The 14 T Conventional Full Adder

Full adder has been derived with various structures previously to reduce the power dissipation and area reduction. To analyze different parameters of the adders we use the 14T full adder as our base structure. The structure shown in Fig 2, uses pass transistor logic for leakage and area reduction [7]. However still having less number of transistors and reduced leakage, the 14T adder suffers from active power.

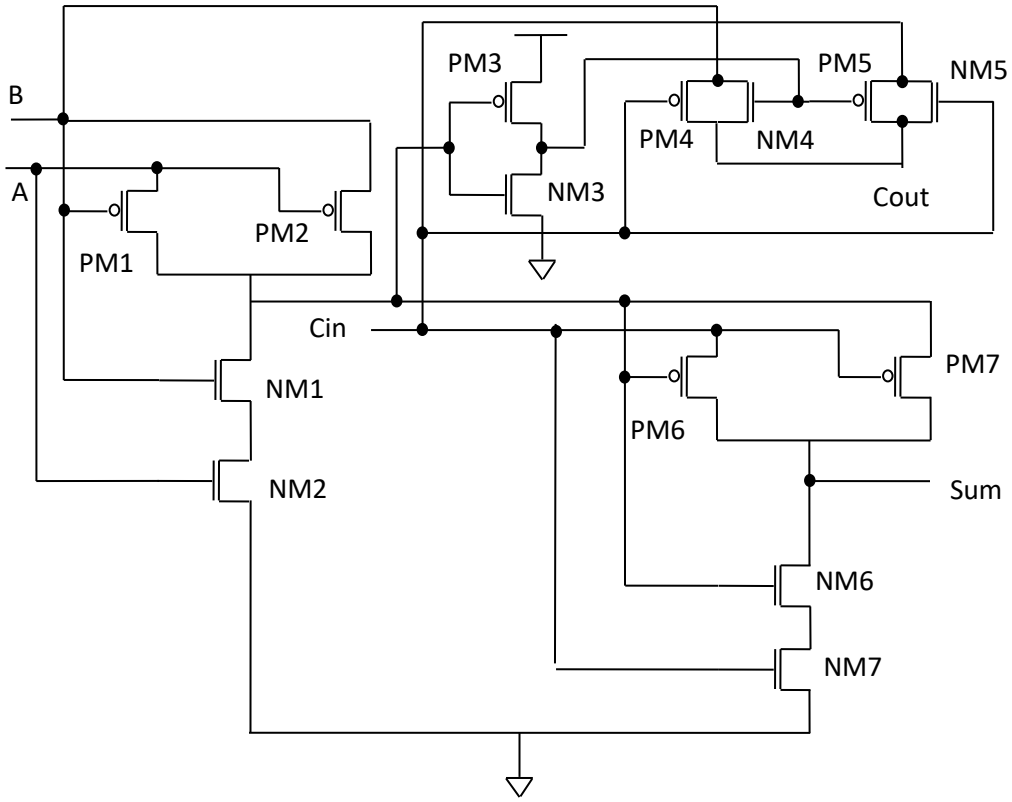

Fig.2. Conventional 14T Full Adder.

3 Proposed Tunnel FET Based Adder

Cadence Circuit Simulator SPECTRE incorporates a very accurate two-dimensional physics-based model for double-gate TFET employing evanescent mode analysis. This model is properly calibrated with findings from TCAD simulations and parabolic technique [8], as published in our prior work [9]. Characteristics are obtained by simulating the potential, electric field, and drain current analytical formulas in Verilog-A using SPECTRE. The device is biased for simulation, as Fig. 3(a) illustrates. Fig. 3(b) displays a comparison of the integrated and analytical model's output current charts. The integrated model was first created as an N-TFET and was then slightly altered to create a P-TFET model. The basic logic gates are constructed and simulated using these two models, which are part of the library. The TFET-based adder operates effectively at a drain voltage of 1.2V, and to verify the device's operation, the gate voltage is swept between -1V and +1V. As illustrated in Fig.4.

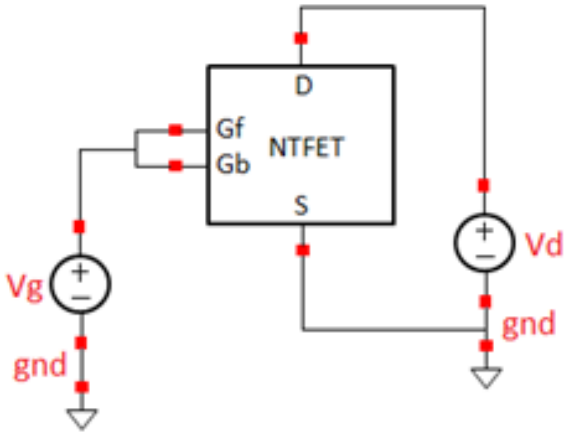

Fig. 3 (a) Schematic of biased NTFET device

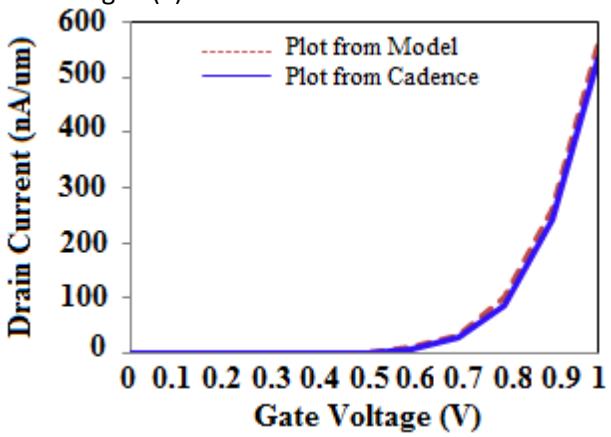

Fig. 3 (b) Characteristics between Drain characteristics

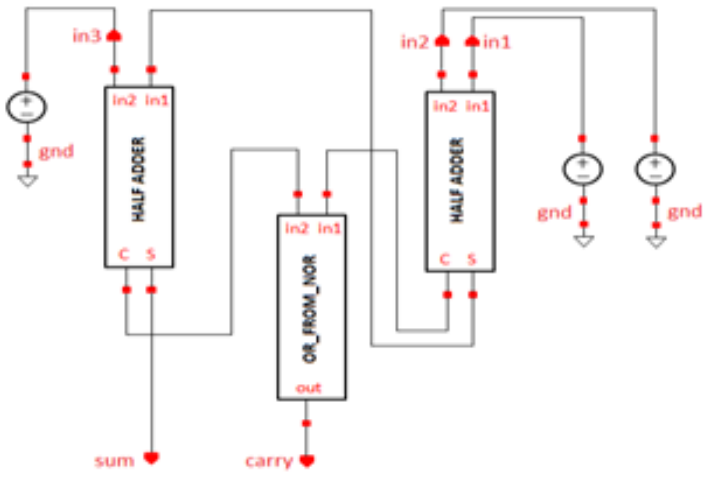

Fig. 4 (a) Schematic of TFET based full adder circuit

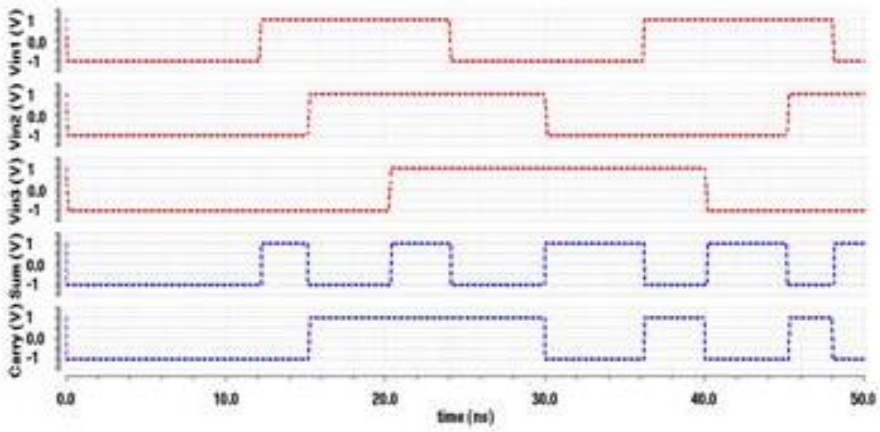

Fig. 4 (b) Simulation result of TFET based full adder circuit

3.1 ACTIVE POWER

The Active power is dissipated by the circuit when the circuit is operation state. Here we will calculate the active power of the circuit at basic of voltage and temperature for the nanoscale technology .The Active power have include both dynamics and static power. The Active power consumption of Transistor circuit [10-11] is consumed by the following equation.

$$Pactive = Pdynamics + Pstatics \quad (2)$$
$$= Pswitch + Pshort + Pleak \quad (4)$$
$$P = fcVdd2 + fIshortVdd + IleakVdd \quad (5)$$

As shown the table I in the case of modified adder based TFET with stacking power gating active power is reduced compared to conventional 14 T adder Based MOSFET. The reduction almost 47.07% at voltage 0.7 V and temperature 27° C.

TABLE 1

ACTIVE POWER DISSIPATION OF 14T ADDER

Circuit	Conventional 14T Adder based MOSFET(nW)		Modified Adder based TFET (nW)	
Active power	1.2 V	27° C	1.2 V	27 °C
	68.02	68.02	32.02	32.02

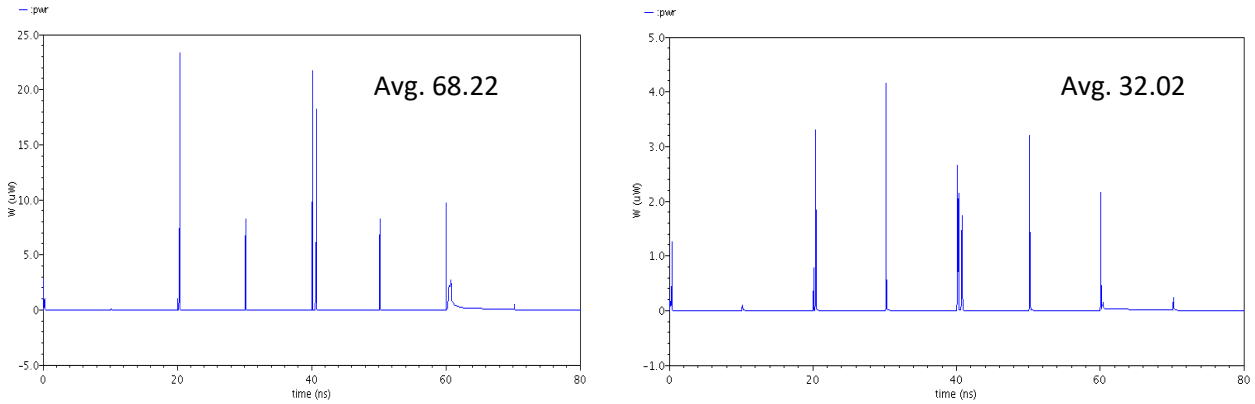

Fig.5(a) Active power wave of conv. 14T (b) Active power wave of modified adder based on TFET

4.CONCLUSITION.

A physics-based analytical model for TFET is integrated in Cadence Analog Design Framework. A library is created to include the integrated device along with basic logic gates based on it. This library is further used to design adder circuit. The active power is reduced up to 47.07 %. The proposed modified adder based TFET is operated at various voltages and various temperatures.

ACKNOWLEDEMENT

This work is supported by Rama University Kanpur in collaboration with Silvaco and Cadence virtuoso Design System, Bangalore India.

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