Design and Analysis of Novel Tunnel Field-Effect Transistor for Biosensor

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Abstract:

Here we present a Tunnel field-effect transistor (Tunnel FET) with asymmetric spacer in this study to achieve high on-current and reduced inverter latency at the same time. Electrical properties of the proposed Tunnel FET are examined using technology computer-aided design (TCAD) simulations with calibrated tunnelling model parameters in order to investigate the proposed Tunnel FET. The symmetric spacer is used to examine the effect of spacer values on tunnelling rate. The on-current increases as the spacer value increases because the fringing field via the spacer increases tunnelling probability. On the drain side, however, the fringing field through the drain-side spacer boosts ambipolar current and gate-to-drain capacitance, lowering leakage and switching responsiveness.

Keywords: Tunnel FET; high-κ spacer; subthreshold swing; band-to-band tunneling
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1. Introduction

MOSFETs have played a critical part in the development of most integrated circuits while reducing their size during the last half-century by scaling their size down to nanometers. As the size of MOSFETs shrank decade by decade, integrated circuits based on them became quicker and more power efficient than their predecessors [1]. In order to reduce the power density, the MOSFET was scaled down, which resulted in a drop in the operational supply voltage. In line with Moore's Law [1,] transistor dimensions have been progressively scaled down over the past few decades to make switching speed quicker and enhance integration density. Device scaling, on the other hand, causes a slew of problems. Short-channel effects (SCEs) and high leakage current are two examples. To address these issues, traditional planar metal oxide semiconductor field-effect transistors (MOSFETs) are being replaced by multi-gated (MG) FETs (e.g., FinFETs), which have superior gate controllability and hence a higher on/off current ratio with better SCEs [2]. Various device designs have recently been investigated as potential next-generation devices beyond FinFET [3–7]. Because most portable electronic devices require low power consumption to keep them working for a long time, steep subthreshold swing (SS), which causes low supply voltage operations, is one of the main challenges. One of the options for SS of less than 60 mV/dec is the tunnel field-effect transistor (Tunnel FET). In contrast to MOSFETs, which have SS limitations (>60 mV/dec) due to thermionic emission at ambient temperature, tunnel FETs employ band-to-band tunnelling (BTBT) as a carrier injection method. An n-type tunnel FET has a p-type source, intrinsic channel, and n-type drain, and is thus compatible with a traditional MOSFET process because only the source dopant type is

different. In comparison to MOSFETs, it has a low leakage current and temperature sensitivity. It also has a reduced on-current due to a narrow tunnelling zone with high tunnelling resistance[4-6].

To increase the on/off current and switching speed, a silicon tunnel FET with high and low spacers on the source and drain sides, respectively, is proposed. Using a high-spacer in a typical tunnel FET (i.e., no line-tunneling) to enhance on-current is not an effective solution because the fringing field depletes the source energy band, resulting in high tunnelling resistance [23,24]. To enhance the tunnelling current, more source-to-channel junction optimization or a low-spacer is necessary. Fringing field effects, on the other hand, boost the tunnelling current in tunnel FETs with line-tunneling without any junction optimization[8-12].

2. Device Structure and Parameters

The semiconductor tunnel FET construction utilized in the simulations is shown in Figure 1. To improve gate controllability and tunnelling current drivability, a double gate and tunnel area underneath the gates has been added. The tunnel area thickness is 4 nm, while the source overlap length is 20 nm.[11-15].

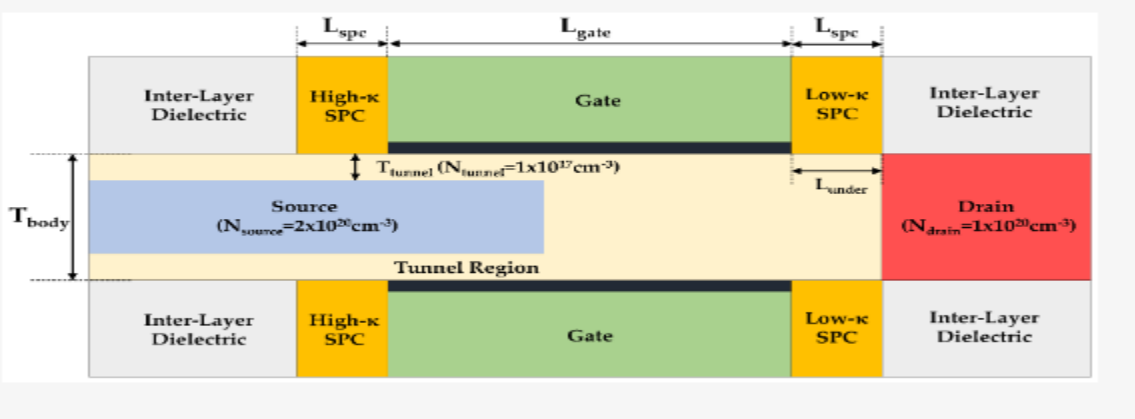


Figure1. The schematic of the proposed tunnel field-effect transistor (FET), which have double gate, asymmetric spacers, and a tunnel channel region to improve the tunneling current.

3.Simulation result and proposed Tunnel FET

Figure 2a depicts the transfer characteristics of various spacer values while maintaining a thickness of 10 nm. 3.9, 7.0, 9.0, 15.0, and 25.0 are the values of spacers, which correspond to SiO2, Si3N4, Al2O3, Y2O3, and HfO2, respectively [28]. Because tunnelling mostly occurs between the source and tunnel area beneath the gate, without the effects of the fringing field through spacers, drain current is independent of values in the subthreshold zone (0.0 V VGS 0.35 V). Drain current begins to grow with rising VGS value starting at 0.35 V. The output characteristics, as illustrated in Figure 2b, also exhibit improved current drivability. When VDS = 1.0 V, the drain current with the spacer = 25.0 is more than two times higher than when VDS = 1.0 V. The spacer has a value of 3.9. The BTBT rates in the channel region underneath the spacer are evaluated to see if the high-spacer improves performance. Figure 3a shows the two-dimensional (2D) electron tunnelling rate contour with a spacer of = 3.9 and 25 at VDS/VGS = 1.0 V/1.0 V at VDS/VGS = 1.0 V/1.0 V. In the case of 3.9, the incidence of tunnelling in the channel under the spacer zone is small (dashed red square).

Table 1. Structure dimensions used in technology computer-aided design (TCAD) simulation.

Definition	Parameter	Value
Gate Length	L_{gate}	100 nm
Equivalent Oxide Thickness	T_{ox}	1 nm
Spacer Thickness	L_{spc}	0–10 nm
Spacer Dielectric Constant	κ_{spc}	3.9–25
Body Thickness	T_{body}	20 nm
Tunnel Region Thickness	T_{tunnel}	4 nm
Drain Underlap Length	L_{under}	10 nm
Tunnel Region Doping	N_{tunnel}	1×10^{17} cm^{-3}
Source Doping	N_{source}	2×10^{20} cm^{-3}
Drain Doping	N_{drain}	1×10^{20} cm^{-3}

This suggests that silicon oxide does not provide a strong enough fringing field to boost tunnelling probability. When a spacer with a value of 25 is applied, however, the fringing field under the spacer region increases, indicating significant tunnelling frequencies.

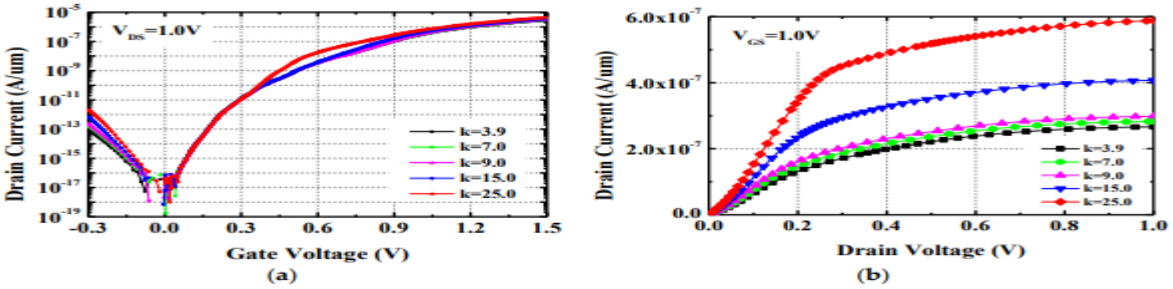
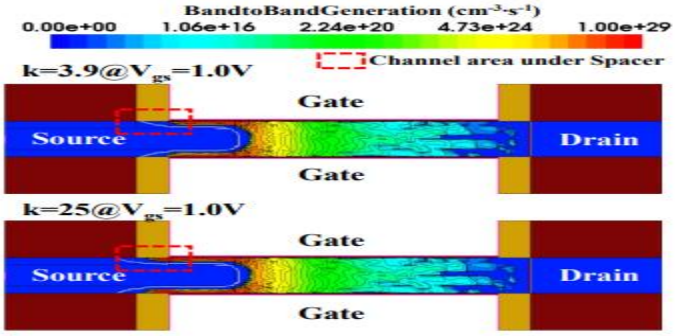
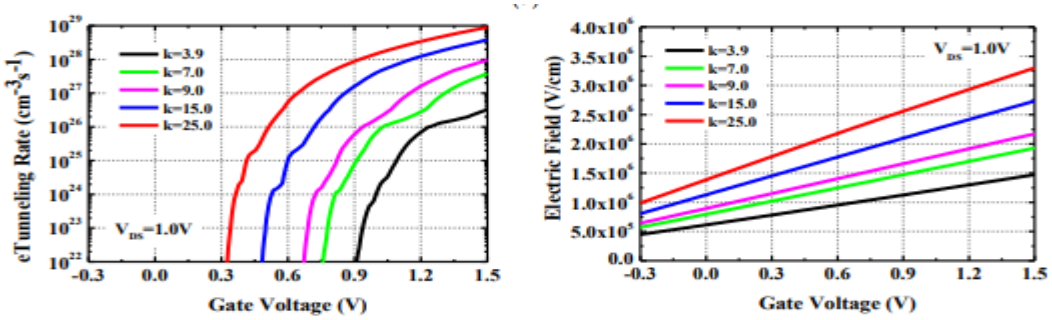


Figure 2. (a) Transfer characteristics at VDS = 1.0 V (b) output characteristics at VGS = 1.0 V with different κ values of spacers.

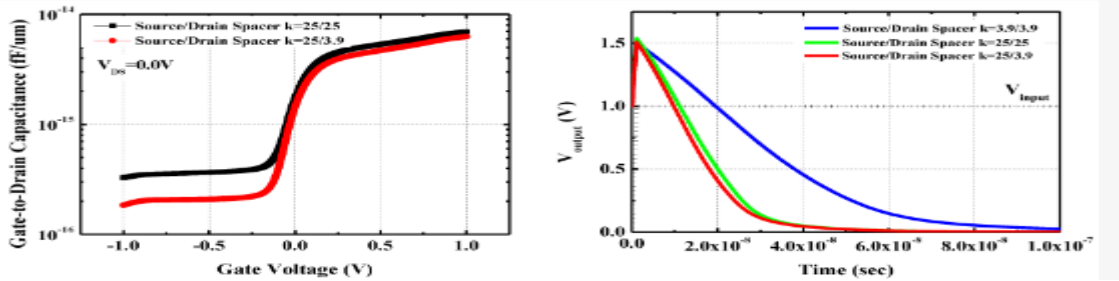


(a)



(b) (c)

Figure 3. (a) Two-dimensional (2D) contour mapping of electron tunneling rate at VGS = 1.0 V for the spacers with κ = 3.9 and κ = 25. (b) Averaged electron tunneling rate, and (c) averaged electric field at VDS = 1.0 V in the channel region under the spacer.



(a) (b)

Figure4. (a) Gate-to-drain capacitance-voltage characteristics at VDS = 0.0 V with symmetric high-κ spacer (κ = 25) and asymmetric high/low-κ spacer (κ = 25/3.9). (b) Inverter response characteristics with symmetric low-κ spacer (blue), symmetric high-κ spacer (green), and asymmetric high/low-κ spacer (red).

The averaged electron tunnelling rate in the particular region under the spacer is shown in Figure 3b. Tunneling generated by the fringing field begins at VGS = 0.31 V and continues to rise in the case of = 25. Tunneling is formed by the fringing field at the bigger VGS as the values get smaller. The low fringing field even starts from VGS = 0.9 V for = 3.9. The tunnelling turn-on voltage difference between = 3.9 and = 25 is nearly 0.6 V. Based on these findings, it is clear that high-spacer devices are better suited to low-power and high-performance applications. In Figure 3c, the averaged electric fields beneath the spacer are also examined for different values, where the electric fields linearly rise as a function of time.As illustrated in Figure 5, the suggested tunnel FET construction may be incorporated. For the asymmetric spacer method, oxide/poly-Si are progressively deposited on silicon-on-insulator (SOI) wafers (Figure 5a). The low-spacer is created using deposition and etching after the drain-side is opened by photolithography and etching. Then, using the ion implantation method, a self-aligned drain is defined (Figure 5b). Oxide is deposited over the whole area to passivate the drain side during following procedures, and the oxide planarization is accomplished using the chemical mechanical polishing (CMP) technique. After the poly-Si is totally removed using chemical etchant, a nitride spacer is produced on the oxide as a hard mask for the line tunnelling area under a portion of the gate region (Figure 5c). The oxide and partial SOI etching are done in order, and the source area is implanted with an ion. The selective epitaxy growth (SEG) layer, which can improve tunnelling current, can be deposited without doping on the partly etched SOI area (Figure 5d). Dopant activation is then adjusted,

and nitride spacer creation is used to calculate the line tunnelling region with self-alignment. Then, to enhance the tunnelling current, a source-side high-spacer is produced (Figure 5e), and oxide is coated and planarized as an interlayer dielectric (ILD). Finally, nitride and oxide are etched off selectively and replaced with ALD interfacial oxide, a high-insulator, and a metal gate (Figure 5f). BEOL flows are omitted since they are identical to ordinary complementary MOS (CMOS) flows.

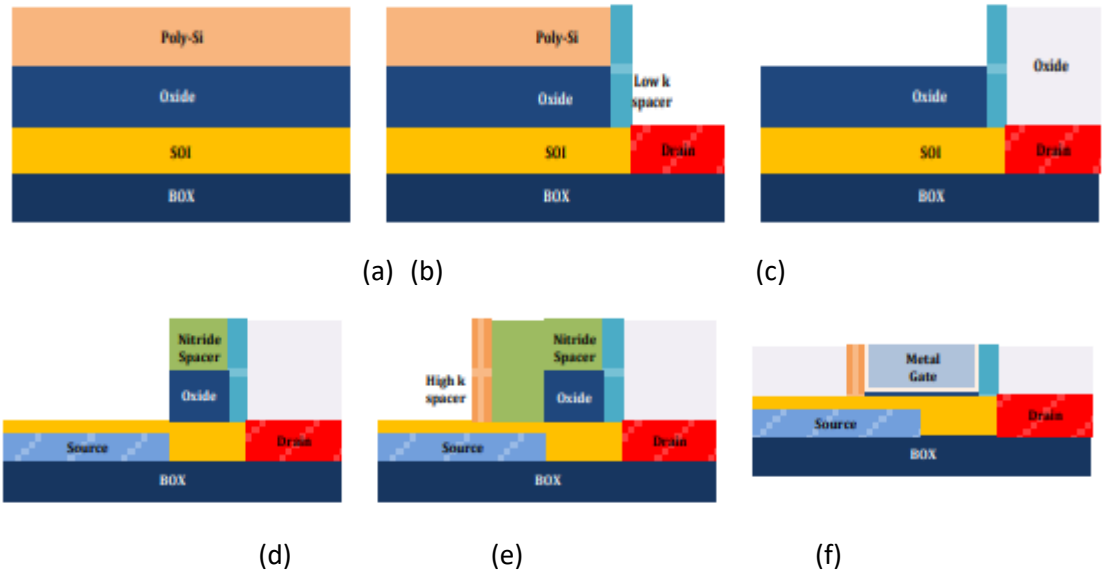


Figure 4. Process flow for the proposed tunnel FET with asymmetric spacers. (a) oxide and poly-Si deposition on SOI wafer. (b) drain-side patterning by photolithography and etching, low-κ spacer and drain region formations (c) oxide passivation on drain-side and poly-Si removal. (d) based on nitride spacer formation, oxide and partial silicon etching, then source region and channel epitaxy formation. (e) nitride and high-κ spacer formations. (f) oxide passivation on source-side and highκ/metal gate.

4. Conclusions

Using TCAD simulations, the tunnel FET with asymmetric spacers is suggested and examined in comparison to the symmetric spacer. Although the high-spacer produces a huge fringing field and enhances on-current, it has downsides, including a rise in ambipolar current and gate-to-drain capacitance. The asymmetric spacer is used to overcome these drawbacks, and it can minimise ambipolar current and gate-to-drain capacitance by reducing the fringing field between the gate and drain. As a consequence, the switching properties of the tunnel FET with asymmetric spacers may be improved by 52 percent. In addition, the manufacturing flow of the suggested tunnel FET is described in terms of process feasibility, taking into account CMOS compatibility.

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