A modified SVPWM for Z Source NPC Three-level inverter fed Induction motor drive

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Abstract:

This paper presents an modified space vector PWM for Z Source Multi level inverter, By using single impedance (Z) network and respective Shoot Through (ST) switching States. Nevertheless, the states of ST limits the modulation index and causes a huge ST current in the inverter phase legs. The Z networks are directly responsible for balancing the inductive boosting voltage and output levels. The existing methods use the full ST which occupies the more switching commutations per cycle and it leads to unequal charging and discharging of inductor, causes more harmonics in the output voltage and currents. This work proposes a development of an enhanced SVPWM technique to balance the charging and discharging of inductors of Z network with DC link capacitors. The proposed method performance has examined with induction motor drive and it is validated in simulation environment

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1. Introduction

To meet the industrial needs and power utilities, three phase induction motor (IM) drives are widely used, as they have very good speed-torque characteristics. A silicon carbide/gallium nitride based fast switching devices are used to design the variable frequency drive (VFD) system [1]. Inverter plays a significant role in the drive performance. In this context the Z-source inverter is an emergent power electronics converter topology for DC to AC conversion with buck-boost characteristics [2]. The Z-source converter circuitry uses two identical structures, X-shaped capacitance and inductance, impedance network connected between DC input source and inverter circuit for enhancing its AC output voltage. From the MLI family, the NPC –MLI is a suitable topology to embrace the full circuit and operation characteristics of conventional two-level inverter. The three-level converter was first proposed by Nabae et al., in 1981 [3]. The NPC-MLI is also called as Diode clamped (DC) MLI, since it uses the diode to clamp the input DC voltage according to the level requirements [3-4]. As for conventional two-level VSIs, NPC-MLI can only step down (buck) their output voltage, which at times, can be a limitation when they are used for interfacing renewable sources whose output voltages may fluctuate continuously. While developing the MLI through Z source network, it provides both the MLI and Z source network benefits. Hence, the Z source connected MLI is very attractive in industry and PV applications [5-9]. In continuation, the work is extended in Z source MLI and developed variety of PWM methods for controlling the Z-MLI in different aspects of input shoot through (ST) switching to improve the performance of the inverter and circuit reliability [10-13]. Recently, much attention in new Z source network design for low-voltage applications such as T-Source , L-source, Y-source, Trans-Z-source, LCCT-Z-source and transformer-isolated source etc., and these topologies are classified mainly into two categories namely isolated and non-isolated [14]. These Z source topologies are provide freedom for the voltage gain extension in higher level. However, development of PWM for these topologies are still challenging as it has a controllability to operate the inverter in high efficiency with degree of freedom for their buck-boost [15-18]. Hence, still require the significant developments in PWM methods for Z source MLI, particularly to improve the output voltage profiles. The sinusoidal PWM and space vector PWM are the two key PWM schemes to handle inverter in a more fruitful way. In particular, MLIs are much benefitted while using space vector PWM, since it provides an opportunity to alter the switching events to improve the inverter

performance [18].

The space vector PWM is a prominent modulation technique for MLIs which can accomplish the following characteristics: (i) it offers a number of redundant switching states and (ii) it gives a freedom to select switching states as well as their switching sequence [11,17]. However, due to the profound theory, the implementation of space vector PWM is complex. The complexity is because of the difficulty in finding the position of voltage reference vector (V_{ref}), and their switching selection and on-time calculations. The concept of space vector PWM is first introduced by Dae-Wook-Kang et al., in 1999 [18]. The concept of vector transformation was proposed for implementation of space vector PWM by Celanovic et al., in 2001 [19]. Furthermore, in a real-time implementation, it does not allow for a methodical manner for identifying the switching [20]. Later, several strategies have been presented for matrix transformation reduction using trigonometric technique. The coordinate transformations system is being used to compute switching on-times and to obtain the V_{ref} . On the other hand, to implement space vector modulation, it is essential to use of higher-end digital controllers due to the numerous mathematical functions required to determine the reference voltage vector coordinates [21].

The multicarrier SPWM (MCSPWM) is a simple method for MLI. Various MCPWM are proposed and each of them are owing pros and cons. Similar to MLI, the space vector PWM and SPWM are the direct choice of the Z-source MLI as well [7]. Nevertheless, SPWM is not a suitable method in Z-source inverter, since it would not give flexibility to alter the ST states. The space vector PWM is a right candidate to handle the ST and non-ST switching in order to control the inverter output. The concept of space vector PWM for Z source MLI was introduced by the Poh Chiang Loh et.al. in 2007 [7]. This utilizes the phase voltage redundancies of the inverter with ST. A scheme for a three-phase three-level Z-source NPC-MLI with reduced number of ST and non-ST states is presented by F. B. Effah et.al [13]. In this method, though the switching states are minimized, the DC-link capacitor balancing is not addressed and the method cannot be applied directly to an n-level Z-MLI. C.Bharatiraja et.al. in 2015 proposed a space vector PWM method which uses standard two-level space vector logic for finding the switching on-times [17]. A shifted SVPWM with simulation and experimental results have been carried out to prove the effectiveness and validity of the scheme using Spartan-3 FPGA [20].

The literature survey given above provides an overview of the work done on space vector PWM development and its implementations. However, it does not have a clear idea in Z-source MLI space vector PWM development and its implementations. Similar space vector PWM performance on Z- source NPC-MLI with voltage-buck and voltage-boost capabilities is investigated with X network for balancing the clamping level to ensure the voltage waveform quality and harmonics performance [10]. Space vector modulation concepts incorporated in Z-source NPC-multilevel inverter would continuously operate with the least number of device commutations per half switching carrier cycle can selectively choose and is configured to switch with a low harmonic distortion. These methods are choosing the nearest switching (nearest three vector (NTV)) in the inverter for the phase current balancing [14]. P. C. Loh et.al [7], [11] uses the same standard carrier-based modulation expressions and are used to mitigate the common-mode voltage including the DC-link balancing [21]-[23]. Even though maximum of Z source topologies can theoretically boost their AC output voltage to any preferred level without any upper limit, the existence of parasitic influences normally reduces the possible gain to a finite (unacceptable) value. These degradations are usually prominent at high duty-ratio high-gain operating conditions, in which the boost inductor is charged over a longer time as well as discharged quixotically at short time interval. Thus, pull out of the high voltage transfer gain from the buck–boost inverters will be difficult in real time practices. In Z-source inverter, the shoot-through switching is related to voltage gain improvement [8]. Although Z-source NPC-MLIs are entrenched and striking solution for medium-power applications, still challenges are there and hence chances exist in voltage profile upgrading, reduction of harmonics, increase in the voltage transfer gain, and decrease switching loss of device etc. Among these issues, topology and shoot-through revision for providing the self-neutral point balancing and reduction of harmonics are viewed as important by default. Although the NPC-MLI is verified to be better for drives application, further adjustments in the PWM strategies and new topology developments in Z-source family can take its application scope to next level. The neutral point voltage balancing is important aspect in NPC MLIs, the SVPWM used for neutral point capacitor voltage regulation [22]. Another method of SVPWM dealt the capacitance charging periods. However this method used the asymmetrical switching which causes the higher harmonics [23]. Hence the devolvement of SVPWM algorithm with neutral point capacitor and reduced of

shoot-through state is applicable for the trials. The modified charging periods of the independent capacitance are to balance their capacitance voltages [24]. Furthermore, explicit voltage and current sensors are not required for detecting any voltage unbalance in the parallel capacitance charging approach since parallel-circuit regulating principles would automatically drive the parallel capacitance voltages to be equal.

Based on the comprehensive literature survey, it is understood that the performance of the Z-source NPC-MLI needs to be improved in the direction of specific drive necessitated claims. There are the varieties of Z-source inverters developed by the researchers for the electrical drives and renewable energy applications. These developments are mainly focused on the voltage gain improvement of the inverter output. The improved voltage gain topology developments and PWM design are the important segments in the electrical drive applications.

The main objective of this work is to develop a simplified reduced shoot-through oriented space vector PWM with voltage boosting operations enhancement and neutral point self-balancing. With this feature, the inverter is providing the self- control on its neutral point, and hence the inverter is able to maintain their output in quarter – symmetry waveform. The proposed scheme can be made into two stages: The First stage is designs a Z-source NPC-MLI, next stage involves the three- level SVPWM with TST and BST for the self-balancing of DC-link capacitors. These investigations were made with nonlinear load such as Induction motor drive. The implementation are carried out for the Full ST, and proposed TST and BST concept based SVPWM using MATLAB/Simulink for 2kW rating Z-NPC-MLI prototype. The proposed implementation is providing the faithful design to reduce the code development time and also permit the flexible implementations.

The structure of the paper is organized as: Section 2 describes the operation of Z Source NPC-MLI and also presents the DC-Link capacitor and phase current effort on neutral point balancing for Z-Source NPC-MLI. The Proposed Space Vector PWM for Z-NPC-MLI and the design produce of the inverter is given in Section 3. Section 4 emphasis on Improved SVPWM based Z-NPC-MLI fed induction motor drive. The corresponding simulation results at different operating conditions are given in Section 5. Finally, conclusions are drawn in Section 6.

2. Z Source NPC-MLI

The Z Source NPC-MLI topology builds with a single Z-source network and neutral point clamped multilevel inverter. The Z source network consists of two inductors ($L_1$and L_2) and two capacitors (C_3 and C_4) associated between the DC input supply and an NPC-MLI circuitry. The NPC-three level inverter consists of twelve power semiconductors with four switches in each phase leg (($S_{a1} – S_{a4}$), ($S_{b1} – S_{b4}$), and ($S_{c1} – S_{c4}$)) and six clamping diodes (D_{a1}, D_{a2}, D_{b1}, $D_{b2,}$ D_{c1}, D_{c2}). The input DC-link is split using two equal DC-link capacitors (C_1 and C_2). These two capacitors are responsible for splitting the input voltage equally ($V_{C1} = V_{DC}/2$ and $V_{C2}= V_{DC}/2$). The circuit diagram depicted in Fig 1. The neutral point voltage between C_1 and C_2 is to be maintained at zero in which NPC circuitry brings the three distinct voltage levels/phase leg. By considering one leg in NPC-MLI, the switching operation of Z-Source NPC-MLI will be similar to the conventional NPC-MLI in the non-ST mode. It is described by three switch options; 1(both upper switch ON), 0(middle switch ON),-1(both lower switch ON). During the ST state, the MLI legs are short circuited for charging of two inductors (L_1 and L_2) to boost the input voltage via Z-network. The summarized switching states illustrated in Table 1 and its description is given in the following section.

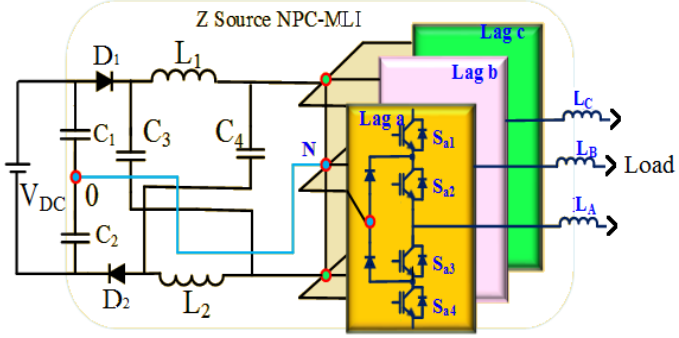


Figure 1. Schematic Diagram of 3 Phase 3-level Z-Source NPC-MLI

Table 1 Switching table of Z source NPC-MLI with NST and Full ST

Mode	Switching State	Tuned on switches	Action	V_{out}
NST mode	+1	S_{X1} S_{X2}	-	$(V_{DC}/2)+L_1*(d_i/d_t)$
	0	S_{X2} S_{X3}	-	0
	-1	S_{X3} S_{X4}	-	$-(V_{DC}/2)-L_2*(d_i/d_t)$
ST Mode	Full ST	S_{X1} S_{X2} S_{X3} S_{X4}	Charging L_1 & L_2	0

Where x indicates lag name (a,b,c)

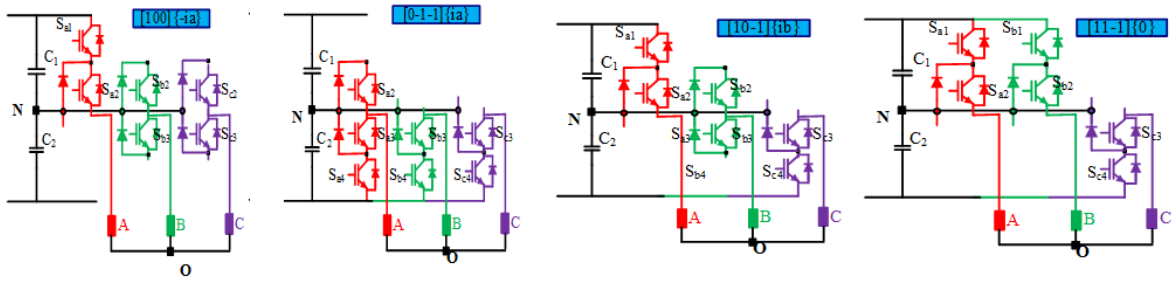
2.1 Switching operation of Z Source Inverter.

The Full Shoot Through(FST) state (where all the four switches are 'ON' in an inverter leg) is able to charge both inductors (L_1 and L_2) simultaneously, however it looses the uniform charging and discharging profile of the Z source capacitors. These inductors with independent control of charging and discharging is capable of maintain the uniform capacitors charging and discharging. During the FST state, voltage across output terminals is zero.

During the non-ST mode, the input DC-link voltage and the inductor voltage together are fed to the inverter which leads to the boosting of the input voltage. The Non-shoot through mode is divided into three states. The positive output voltage can be achieved by triggering S_{a1} and S_{a2}, however this state can be achieved by triggering of only switch S_{a1}. Two switches are turned ON to provide the freewheeling path during the transition of states from 1 to 0. The negative output voltage is produced by triggering S_{a3} and S_{a4}. Similarly, the 0 and -1 state can be achieved by only S_{a3}. At this juncture, the two switches are triggered to provide the freewheeling path during the state transition from -1 to 0. The zero output voltage is achieved by triggering S_{a2} and S_{a3}, which connects the supply neutral point (NP) to the load resulting in zero potential.

2.2 DC-Link Capacitor and Phase Current Effort on Neutral Point Balancing

The DC-link neutral point is a floating point between input capacitor where the potential will change based on the inverter switching. In DC-link, each capacitor ($V_{C1}$and V_{C2}) should be charged to $V_{DC}/2$ and henceforth the capacitor sum of voltages must be equal to the DC-link voltage (V_{DC}). However, in particular operating condition due to the flow of phase current through the neutral point and these capacitor voltages are not identical. This is called as DC-link neutral point fluctuation or capacitor imbalance. This section explains the capacitor imbalance problem for the different inverter switching states. The DC-link neutral point fluctuation is normally happening for inverter regular switching events. According to the SVPWM technique for three-phase three-level Z-source NPC-MLI has 27 switching cases, which are grouped as zero, small, medium, and large. At small and medium switching states the phase currents are given in Table 2. The Figure 2 shows the some into all switching vectors i.e small vector switching event [100], [0 -1 -1], medium vector [1 0 -1] and large vector event [1 1-1] along their phase currents with respect to neutral point. Acquire with states [000] [-1-1-1] and [111] due to the absence of phase currents whereas the states like small and large switching options are involve active participation of reference point in the phase current as indicated.



(a) (b) (c) (d)

Figure.2 Z-source MLI with different active switching states with their phase current
(a) –ve small vector[1 0 0],(b) +Ve small vector [0 -1 -1],(c)medium vector [1 0 -1],(d)Large vector [1 1 -1]

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Table 2. Phase currents of different switching states

positive small vector switching	i_N	Negative small vector switching	i_N	medium vector switching	i_N
[0 -1-1]	i_a	[1 0 0]	$-i_a$	[1 0-1]	i_a
[-1 0-1]	i_b	[0 1 0]	$-i_b$	[0 1-1]	i_b
[0 0 -1]	i_c	[1 1 0]	$-i_c$	[-1 1 0]	i_c
[0 1 1]	i_a	[-10 0]	$-i_a$	[-1 01]	i_a
[1 0 1]	i_b	[0 -1 0]	$-i_b$	[0 -1 1]	i_b
[-1-10]	i_c	[0 0 1]	$-i_c$	[1 -1 0]	i_c

In Z-source NPC-MLI, each and every switching condition is creating the individual phase current, which affects the DC-link capacitors or neutral point balancing. Considering, [100] state as shown in Figure 2, the a-phase is connected to DC-link directly, whereas b and c phases are connected with DC-link neutral point 'N'. To balance the three-phase connected circuitry DC-link, the neutral current (I_N) should satisfy the balance equation $I_N = i_a+i_b+i_c$. The I_N is necessarily becomes zero. Henceforth, $i_b+i_c=-i_a$. Likely, the other states [-1-1 0] and [-1 0-1] are producing i_c and i_b currents respectively, which affects the DC-link balancing.

All of the positive small vector switching and medium vector switching involve the operation of connecting the positive phase current, which discharge the upper DC-link capacitor (C_1). Hence, V_{C1} will rise whereas V_{C2} will decline. Similarly, when the negative phase-current flows through the DC-link neutral point (NP), C_1 is charged and lower capacitor (C_2) is discharged. Table 3 illustrates the understanding of the conditions of DC-link capacitors C_1 and C_2 related to phase positive and negative currents. From the table, the DC-link unbalance mainly depends on the path of the phase current which chooses the charging and discharging status of the DC -link capacitors. Considering the three-phase three-level Z source MLI, it has twenty-seven active switching options (three zero, twelve small, six medium, six large). Out of these, zero and large switching states are not generating the phase current and not affecting the DC-link neutral point balancing. However, the rest of the small and medium switching could influence by the phase current which affect the neutral point balancing. Hence, the balancing opportunity can be established through the effective use of small vector (SV) switching with eliminating the medium vector switching. Twelve switching states result in six small SV pairs. Table 3 illustrates the relation of neutral point and phase currents for the different switching states of the Z-source NPC-MLI. Here the small vector switching is categorized into positive and negative vector switching, whereas all medium vector switching is called positive vector switching.

Table 3 The phase current according to switching vectors

Type of switching vector	**Phase current > 0**	**Phase current < 0**
Positive small vector switching	Charges C_1, Discharges C_2	Discharge C_1, Charge C_2
Negative small vector switching	Discharge C_1, Charge C_2	Charges C_1, Discharges C_2
Medium vector switching	Charges C_1, Discharges C_2	Discharge C_1, Charge C_2
Large vector switching	No change in charging	No change in charging
Zero vector switching	No change in charging	No change in charging

Each small vector switching comprises of double repeat switching options (redundant states) and

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they are leading the even consequence on both DC-link capacitors. While using large and zero vector switching, the phase currents turn out to be zero which maintain the balancing of DC-link capacitors. Alternatively, medium vector switching directly affect the phase current and leads to DC-link neutral point, as they do not have any redundancy to the maintain the DC-link capacitors charging and discharging. For proper operation of Z-source NPC-MLI, the DC-link capacitor voltages must be equal ($V_{DC}/2$). The output voltage and current are referred to the DC-link voltage. The NP fluctuation (NPF) is calculated as;

$$NPF = \frac{(\frac{V_{DC}}{2}) - V_{C1}}{V_{C1}} \quad (1)$$

3. Development of improved Space Vector PWM for Z-NPC-MLI

The tremendous identified feature of SVPWM is that flexible handling of the shoot through states of Z-NPC-MLI. On basis of it SVPWM is optimum option for Z-NPC-MLI. This section describes the conventional SVPWM and Improved SVPWM scheme for Z NPC-MLI.

3.1 Conventional SVPWM for Z-NPC-MLI

Similar to conventional MLI, the Z -source MLIs space vector diagram require sectors, triangles, and switching vectors with shoot-through switching vectors which are responsible for boosting the DC-link voltage for the inverter. The Z-Source NPC-MLI need shoot-through vectors to charge the Z-network inductors. In ST period the four switches in a single leg are turned on for a small period which is called as full shoot through mode (FST). The space vector hexagon formed with 27 switching vectors, among which 3 for Zero Vectors, 12 for Small Vectors, 6 for Medium Vectors and 6 for Large Vectors [10]. The space vector diagram is shown in fig.3.

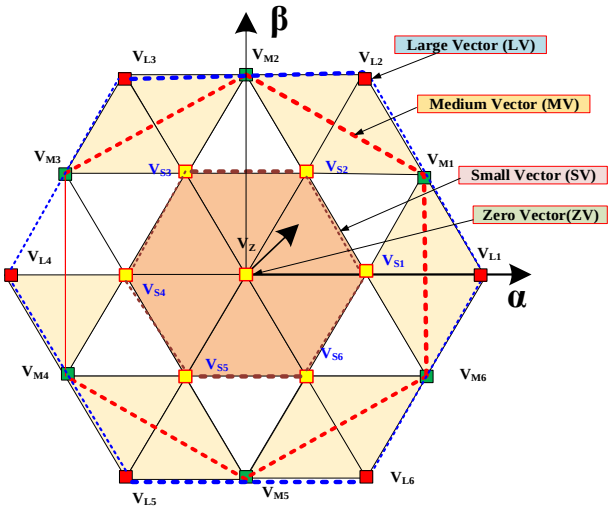

Figure 3: Space Vector diagram of Z-NPC- three level inverter

The FST can be done in any phase of the inverter similar to two-level inverter. However, in practice the shoot through mode is created based on the nearest three vector (NTV) method which helps the inverter switching stress and DC-link balance naturally with minimal switches. In this method, the inductors (L_1 and L_2) are charge by using upper and lower switching states. From fig 4 Consider the sector 1, the sub-triangle $\Delta_{1,2}$ switching pattern is {[0 -1 -1], [1 -1 -1], [1 0 -1], [1 0 0], [1 0 -1], [1 -1 -1], [0 -1 -1]} as shown in fig 5. Similarly, switching patterns are considered for remaining sub triangles of sectors.

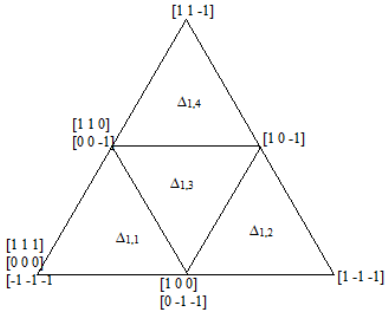

Figure 4: Space vector diagram for Sector 1

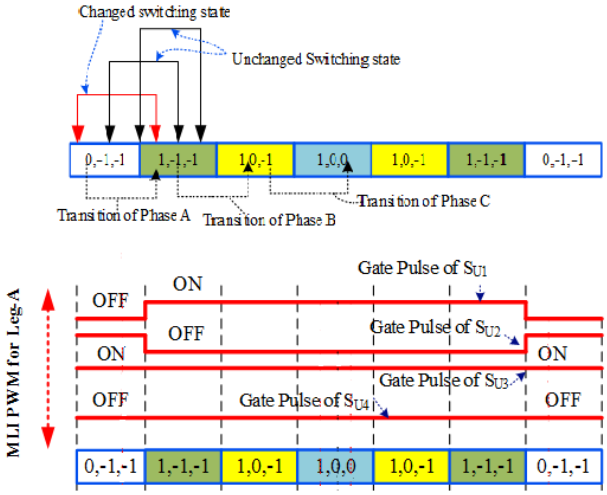

Figure 5: $\Delta_{1,2}$ ST switching state and PWM pulse for Z-NPC-MLI

3.2 Improved SVPWM for Z-NPC-MLI

The SVPWM scheme has been improved by shoot through concept for Z-NPC-MLI, the new ST method called Top-ST (TST) and Bottom-ST (BST). The three upper switches in any leg are turned ON for a small period which is called TST mode and when three lower switches in any leg are turned ON for a small period called as BST mode. Therefore, using TST and BST, 54 additional switching vectors are involved with already existing 27 voltage switching vectors (regular MLI switching vectors). The Table 4 shows the proposed TST and BST modes.

Table 4 Switching table of Z source NPC-MLI with Proposed ST mode

Mode	**Switching State**	**Tuned on switches**	**Action**	**V_{out}**
NST mode	+1	S_{X1} S_{X2}	-	$(V_{DC}/2)+L_1*(d_i/d_t)$
	0	S_{X2} S_{X3}	-	0
	-1	S_{X3} S_{X4}	-	$-(V_{DC}/2)-L_2*(d_i/d_t)$
Proposed ST Mode	Top ST	S_{X1} S_{X2} S_{X3}	L_1 Charging	0
	Bottom ST	S_{X2} S_{X3} S_{X4}	L_2 Charging	0

*Where x indicates lag name (a,b,c)

The Fig. 6 shows the three-level Z-source multi-level inverter space vector diagram. Here, T and B are represented as TST and BST respectively. This shoot-through are created based on the switching transition from 0 to 1 and 1 to -1 and -1 to 0, which are related to DC-link voltage connection to load with phase current generation. The phase current is positive, from 0 to 1 and negative for-1 to 0. For $\Delta_{1,2}$ switch state and PWM gate pulses for inverter leg A for proposed SVPWM based Z-NPC-MLI is shown in fig.7. Similarly all six sectors are created by the help of TST and BST.

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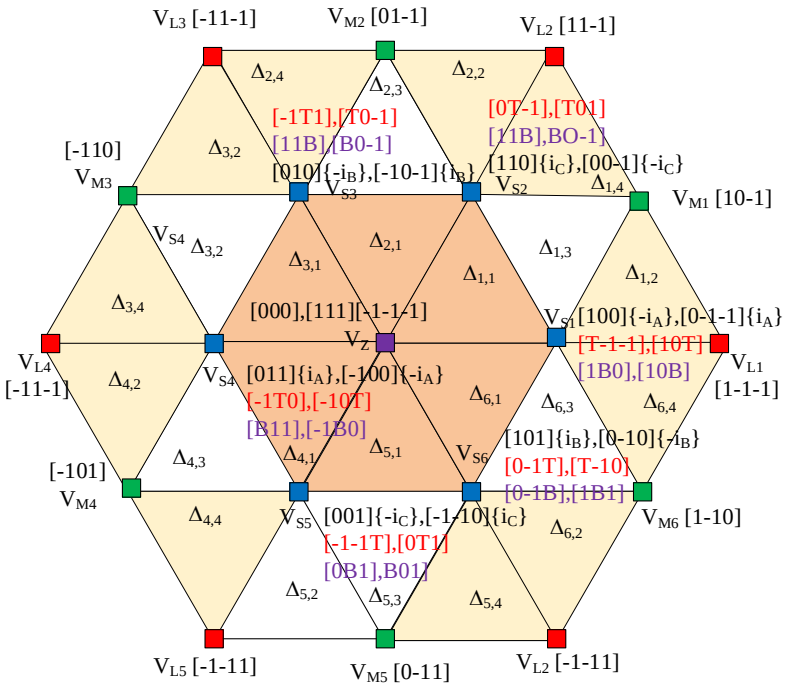

Figure.6 space vector diagram with TBST scheme for Z-NPC-MLI

Creating shoot-through leads to the zero-pole voltage for that respective phase. This will create a disturbance in the machine appliances (load). Improper turning on procedure for creating shoot through leads to higher switching losses because of more switching commutations. Hence, the proper creation of shoot through is necessary to give the boosted output voltage without disturbing the pole voltage or line voltage. To avoid more switching commutations TBST method is preferable as only three switches in a phase are turned on to charge the inductor at preferable locations to eliminate the effects on pole voltage or line voltage during shoot through operation. This ensures a better output quality. The Table 4. shows the possible shoot-through switching options in one full space vector volts-sec balance cycle.

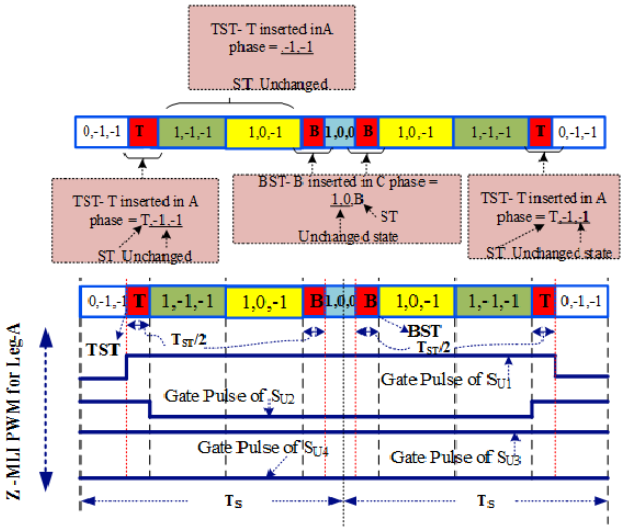

Figure.7 $\Delta_{1,2}$ ST switching state and PWM pulse for proposed SVPWM based Z-NPC-MLI

In the Fig. 8(a)-(d) shows the different modes of operation of Z-NPC_MLI. During the ST mode, the inverter can be involved either full ST or partial ST. Evan though, the both methods are shorting the input DC source via inductors L_1 and L_2, the full ST (FST) is not a best choice of balancing the inductor's charging profile (nonlinearity charging) and it roots the high magnitude of lower order harmonics in the output waveforms. Meanwhile the TST and BST has an individual control on the L_1 and L_2 charging characteristics, the combination of TST and BST maintains the inductors charging in parallel, which ensures the better quality output waveform.

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3.3 Analysis of Z source network

As Shown in fig.1, the inductor is charged by the capacitor during ST time (T_{ST}). The Z source network L_1 and L_2 inductor current ripple ΔI is consider as 10% of inductor current (I_L).

The capacitor and Inductor values are obtained as $L = \frac{VT_{ST}}{\Delta I}$ and $C = \frac{\bar{I}_L T_{ST}}{\Delta V_C}$ respectively.

The average inductor current is $\bar{I_L} = \frac{P_i}{V_{DC}}$ (2)

Here P_i is total power and V_{DC} is the DC –link voltage. The V_L and V_C are the inductors and capacitors voltage respectively,

$V_{L1} = V_{L2} = L(\frac{di}{dt})$ (3)

$V_{C3} = V_{C4} = (\frac{V_{DC}}{2}) = V_C$ (4)

During the Non ST time, $V_C = V_L = V_{DC}$.

In this situation is fulfilled, as the capacitors of Z source network C_3 and C_4 are connected in parallel. Therefore, in ideal conditions the net voltage across the Z source network is $2V_C = V_{DC}$. Where V_L=V_C and the output voltage of the inverter V_o will be zero.

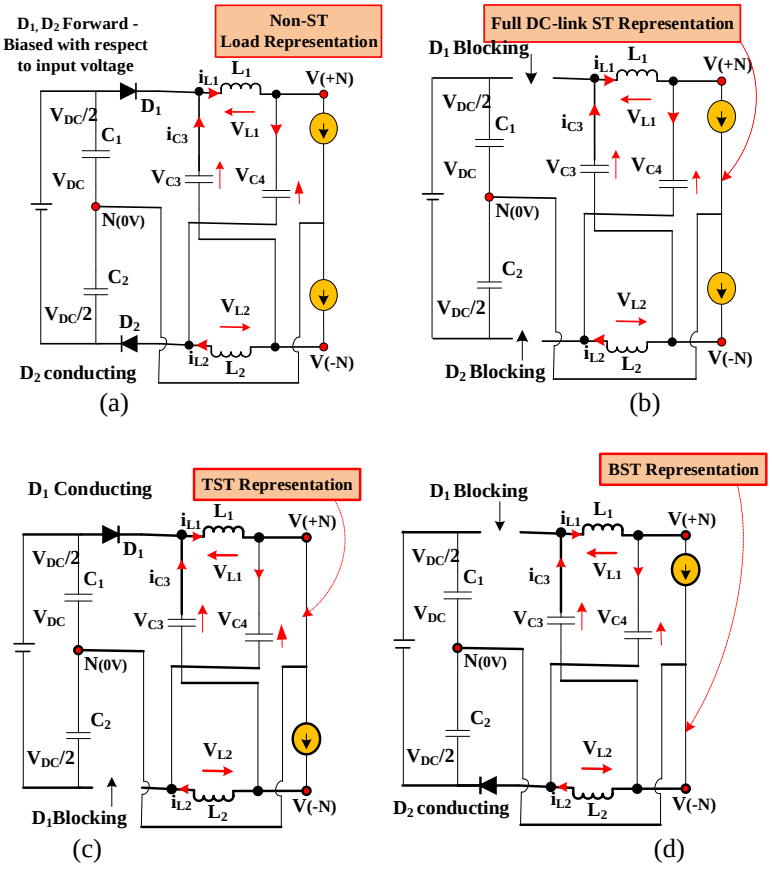

Figure.8 Modes of operation of Z-NPC-MLI at (a). Non-ST (NST), (b).full-ST, (c).TST, (d). BST

During the NST operation (see Figure.8.a) the diodes D_1 and D_2 are in forward bias, the $V(+) \Rightarrow \frac{V_i}{2}$; $V(-) \Rightarrow -\frac{V_i}{2}$. Hence the V_{L1} and V_i is obtained as,

$V_{L1} = V_{DC} - V_C$ (5)

$V_i = 2V_C - V_{DC}$ (6)

In TST mode operation (see Figure.8.c), the D_2 is in blocking and D_1 is in conduction states. Hence, the V_{L1} are attained as,

$V_{L1} = \frac{V_{DC}}{2}$;$V_{L2} = 0$ (7)

Subsequently V(+) side voltage is zero and V(-) will be = $\frac{V_{DC}}{2} - V_{C3}$

In BST mode operation (see Figure.8.d), the D_1 is in blocking and D_2 is in conduction states . Hence, the V_{L1} are attained as,

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$$V_{L1} = 0; \quad V_{L2} = \frac{V_{DC}}{2} \tag{8}$$

The V(-) side voltage is zero and V(+) will be = $-\frac{V_{DC}}{2} + V_{C4}$

In steady state condition, inductors (L_1 and L_2) average voltage in one cycle (T) is zero,

Hence $T_{NST} + T_{TST} + T_{BST} = T$.

$$V_{L1} = \frac{(V_{DC} - V_C) * T_{NST} + \left(\frac{V_{DC}}{2}\right) * T_{TST} + \left(\frac{V_{DC}}{2}\right) * T_{BST}}{T} \tag{9}$$

$$V_C = \frac{V_{DC} * \left(1 - \frac{T_{TST} + T_{BST}}{2T}\right)}{\left(1 - \frac{T_{TST} + T_{BST}}{T}\right)} \tag{10}$$

The inverter DC-link voltage at Non ST, TST and BST modes are obtained as,

$$V_{i\_NST} = \frac{V_{DC}}{\left(1 - \frac{T_{TST} + T_{BST}}{T}\right)} \tag{11}$$

$$V_{i\_TST} = V_{i\_BST} = \frac{V_{DC}/2}{\left(1 - \frac{T_{TST} + T_{BST}}{T}\right)} \tag{12}$$

From the Eqs. (11) and (12), it could understand that the NST time voltage present in the DC-link is twice of TST and BST modes. Henceforth while using TST and BST, the C_1 and C_2 is equally share the input DC voltage which helps to improve DC-link capacitors balancing and THD performance in the output waveform.

The peak AC output voltage of the inverter is consider as, V_{x0}(x={A,B,C}), Hence During the Non ST, TST and BST modes the output voltage is derived and give as,

$$V_{x0} = \frac{M}{\sqrt{3}} V_{i\_NST} \tag{13}$$

$$V_{xo} = \{\frac{M}{\sqrt{3}} V_{DC}\} \frac{1}{\left(1 - \frac{T_{TST} + T_{BST}}{T}\right)} = \{\frac{M}{\sqrt{3}} V_{DC}\} B_F \tag{14}$$

Where B_F is boosting factor ($B_F \geq 1$).

4. Improved SVPWM based Z source NPC-MLI fed induction motor drive

The earlier section describes the proposed TST and BST based SVPWM technique. To overcome the main disadvantage like discrete nature of output which provides path for harmonic disturbances, high switching losses, thermal losses, and bearing failure of machine. The bearing current associated with electromagnetic fields is represented as circulating current and it is influenced by long axial cable, high switching frequency, and common-mode current (CMC) . Another way of bearing current associated with electrostatic fields may result in shaft voltage. The induced shaft voltage may create problem in bearings, mechanical loads, sensors, and position encoders. Electromagnetic interference incorporated with PWM ac drives, which creates an unwanted effect on communication equipments and it leads to malfunctions of control systems. Due to bearing current existence, the life time of the bearing shrinks; thereby, it causes motor failure and it laid to unscheduled maintenance and economic loss for industries. To reduce the bearing currents, fully depended on PWM techniques used in the inverter, Great effort should be devoted to reduce bearing current for effective operation of drives and in NPC-MLI's NP capacitor's lifespan reduces due to the NP fluctuation between the capacitors. Which produce the high voltage and current harmonics and it leads to inferior the drive performance. It deliberately introduces the improved SVPWM to eliminate the bearing currents with respect to the NPC-MLI switching state. The Fig. 9 shows the complete setup of a three-phase three-level Z- NPC-MLI-fed induction motor (IM) drive. The Z-NPC-MLI operates with improved SVPWM switching technique, which gives the specific feature of Z network voltage boosting capability and Low harmonics distortion capability of MLI along with neutral point balancing. In later section, describes the performance of Z-NPC-MLI topology with nonlinear load through simulation and it is validated experimentally.

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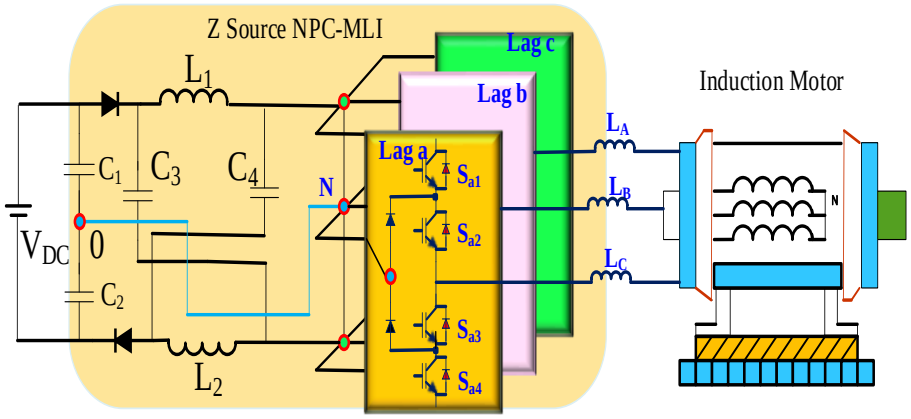

Figure 9: Schematic diagram of 3 Phase 3-level Z-Source NPC-MLI drive

5. Implementation of proposed scheme

The performance of the improved space vector PWM for three-phase three-level Z-source NPC inverter with an adjustable speed induction motor drive is investigated in MATLAB environment. In continuation, the 2kW laboratory scale three-level Z-source NPC inverter fed induction motor experiment has validated.

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5.1 Simulation Results

The MATLAB-Simulink is built to test the performance of the proposed space vector PWM for three-phase three-level Z-source NPC inverter with an adjustable speed induction motor drive. The input DC-Link voltage is fixed maintained as 200V via fixed DC source (AC to DC rectifier). The two DC-link capacitors (C1 and C2) with value of 100 µF placed in the input side of the inverter. The values of capacitance (C_3 and C_4) and inductance (L_1 and L_2) in Z-source network are 470 µF and 10 mH respectively. The twelve IGBTs with a parallel diode for commutation are used as the switch in the circuit. The internal resistance of IGBT is considered as 1mH. The DC-link capacitors (C_1 and C_2) are considered across the supply to split the supply voltage into two equal halves and to create a neutral point. The boosting factor is considered to be B=1.87 as maximum. As per result, when the input DC supply voltage of 200V theoretical output should be 336.6V for 0.9 modulation index (till maximum linear modulation range).

The simulation is performed for all low to higher modulation range i.e M_a = 0.1 to 0.9. The Fig.10 shows simulation results of the line voltage (V_{Line}) at modulation M_a=0.7. Here, the V_{Line} and percentage of THD is observed to be 261.8V and 16.92% respectively. Here, it understand that the V_{Line} found very low at the lower modulation indices because the ST time of the Z-source MLI will be less during this period, and then the V_{Line} gradually increases with the increase of the Ma. Next, the proposed space vector PWM is tested for the extreme linear modulation range (M_a=0.907) the V_{Line} voltage waveforms are shown in the Fig 11. At M_a=0.9, the inverter delivers its maximum output voltage 336.6V with considered harmonics spectra of 17.56%. The table 5 shows the V_{Line} and percentage of THD for the different M_a is given. Based on the results, the output voltage is linearly increased. In addition, the proposed space vector PWM output V_{line} and its respective % THDs are comparatively better when compared to the reported method. The Harmonic spectrum for M_a = 0.7, and M_a = 0.907 shown in fig 12(a) &(b) respectively. The Simulation results given in fig 13(a) &(b) for inverter input DC-link capacitor voltages at M_a =0.7 for TBST mode and FST mode. The Fig 14(b) shows the simulation results of inverter input DC-link capacitors voltage V_{C1} and V_{C2} at M_a =0.9 for FST mode. Here the V_{C1} and V_{C2} are observed as 107.2V and 93.8V respectively. The inverter neutral point fluctuation (NPF) is calculated. The calculated NPF is 7.11% which causes larger fluctuating on the inverter switching. This roots the higher voltage THD on the inverter line voltage. The Fig 14(a) shows the inverter V_{C1} and V_{C2} at M_a =0.9 for the proposed TST and BST . Here the V_{C1} and V_{C2} are measured as 101.6V and 98.4V respectively. Therefore NPF is calculated as 1.72%, which is better than FST switching.

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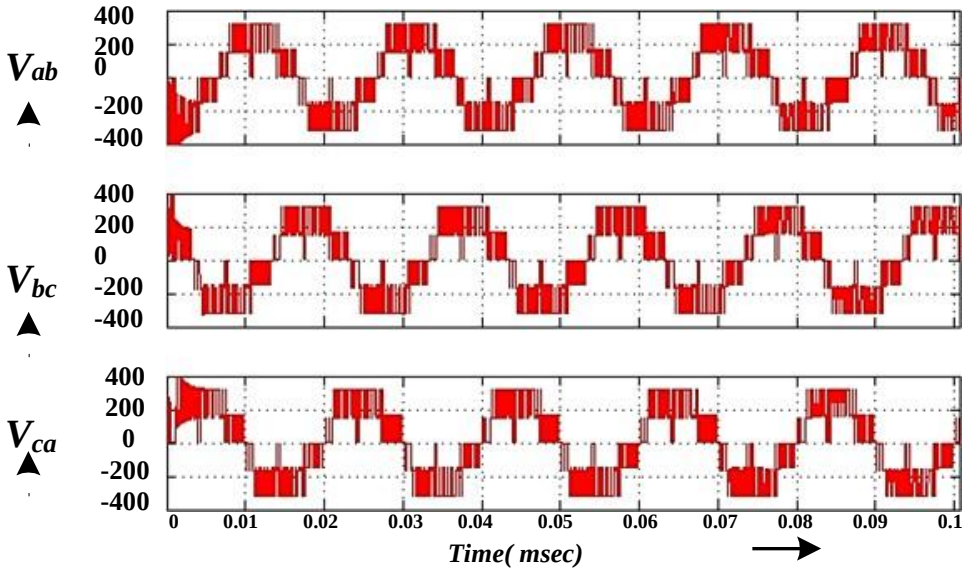

Figure 10. Simulation results a. V_{line} [200V/div] [2ms/div] at $M_a = 0.7$

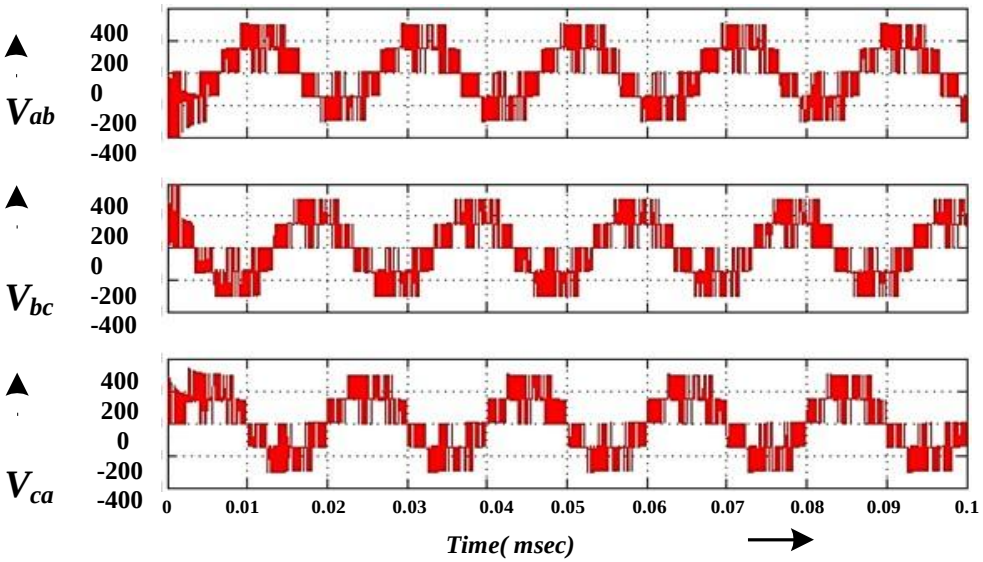

Figure.11 Simulation results a. V_{line} [200V/div] [2ms/div] at $M_a = 0.9$

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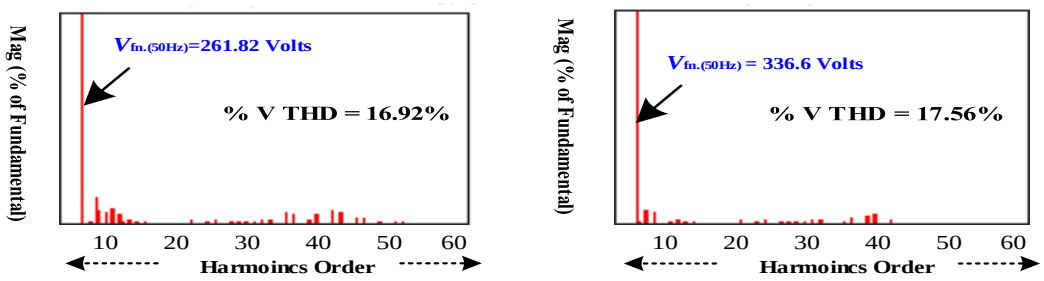
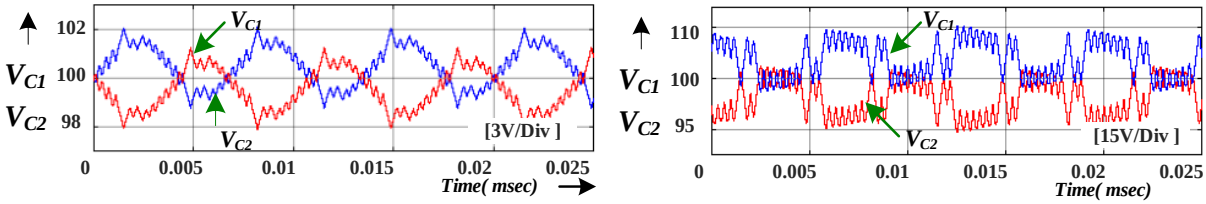


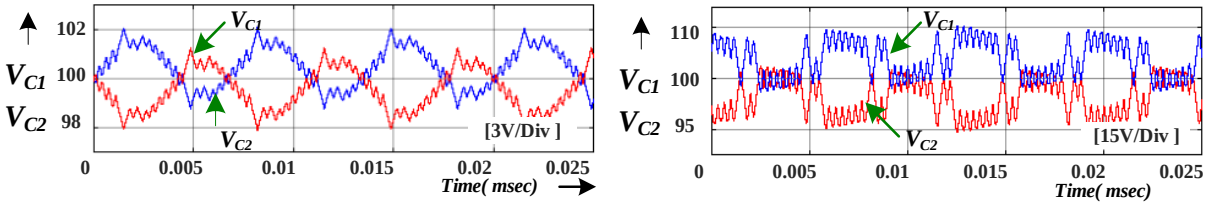
(a) (b)

Figure.12 Harmonic spectrum: (a) M_a = 0.7, (b) M_a = 0.907



(a) (b)

Figure.13 Simulation results of NPC-MLI DC-link Capacitors voltage V_{C1} and V_{C2} at M_a=0.7 : (a) Proposed TST and BST. b) FST



(a) (b)

Figure.14 Simulation results of NPC-MLI DC-link Capacitors voltage V_{C1} and V_{C2} at M_a=0.9: (a) Proposed TST and BST. b) FST

The Table 5 shows inverter performance at different modulation index values for FST and proposed combination of TST and BST switching. The table shows the line voltage, voltage THD and NPF values for the various operating conditions of the inverter.

Table 5. Line voltage, Line voltage THD and NPF for different M_a

Ma	FST			TST and BST		
	V_{Line}(V)	THD in %	NPF in %	V_{Line}(V)	THD in %	NPF in %
0.1	34.5	21.96	6.21	36.5	15.64	1.21
0.2	75.5	20.67	6.52	78.3	15.65	1.62
0.3	109.2	21.95	6.33	111.8	16.62	1.62
0.4	146.1	22.34	6.24	149.0	16.63	1.67
0.5	184.3	23.10	6.25	186.5	16.69	1.68
0.6	224.6	23.54	6.45	224.1	16.72	1.69
0.7	259.3	24.12	7.04	261.8	16.92	1.69
0.8	297.1	27.23	7.06	299.2	17.20	1.71
0.9	334.3	27.62	7.11	336.6	17.56	1.72

Based on the above table it could be understood that FST switching NPF is higher and it is engaged in the range 6.21% to 7.11% However, the proposed TST and BST switching method are maintains the NPF

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value less (between 1.21% to 1.72%). Hence maintains the voltage THD performance better due to betterment of NPF. The simulation results have been confirmed for different operating conditions of the Z-source NPC-MLI against its DC-link capacitors balancing. The advantages of the proposed TST and BST switching method is verified in order to maintain the line voltage harmonics and neutral point balancing. The simulation study and consequences are exhibited to confirm the Z-source NPC-MLI performance upshots.

6. Conclusions

This paper presents modified space vector PWM for three-phase three-level single DC source fed Z –source NPC-MLI drive. In the beginning of the paper, the detailed design and calculation of the ST switching and voltage boosting function is examined. A minimal number of shoot through switching states involved in this work. The proposed SVPWM method effectively associated with TST and BST switching states and phase current flowing at DC-link neutral point. It improves the self-balancing of the DC-link capacitors. The simulation study is conducted through MATLAB/Simulink The simulation results and stated the superiority of the Z source NPC-MLI drive. The proposed method is able to maintain minimal NPF value for all operating conditions, thus eliminated the need of bulky DC-link capacitors and also provide a better harmonics profile and waveform quality, which is suitable for Electric Vehicle applications and Industrial drive applications.

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