Energy- and Area-Efficient VLSI Architecture based MMSE Detector for Massive MIMO Systems

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Abstract

This paper presents a VLSI implementation based MMSE Detector for massive MIMO system scheme for low power. Minimum-mean-square-error (MMSE) detection is increasingly relevant for massive multiple-input multiple-output (MIMO) systems. MMSE suffers from high computational complexity and low parallelism because of the increasing number of users and antennas in massive MIMO systems. The current implementation is based architecture design to iteratively estimate signals. First, a recursive conjugate gradient detection algorithm is proposed that achieves high parallelism and low complexity through iteration. Second, a quadrant-certain-based initial methodthat improves detection accuracy without added complexity is proposed. Third, an approximated log likelihood ratio (LLR) computation method is proposed to achieve simplified calculation. The analyses show that compared with related methods, the proposed RCG algorithm reduces computational complexity and exploits the potential parallelism. RCG is mathematically demonstrated to achieve low approximated error. Based on the RCG method, architecture is proposed in 64-QAM massive MIMO system. The massive MIMO system is designed, implemented and tested in 45nm technology for synthesis and simulation results were carried out from Xilinx 14.3. The proposed architecture with MMSE detector technique has 54 numbers in logic gates and consumes 252 nw in a power dissipation and minimum area of 2010nm.

Index Terms—Massive multiple-input multiple-output (MIMO), detection, very-large-scale integration (VLSI), wireless communications.

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1. Introduction

The number of mobile users is dramatically increasingevery year. Users crave faster Internet access and instantaccess to the multimedia services. In addition, the implementation of smart cities has reached stages wherein a dense and heterogeneous set of devices positioned over the urban area generates Extra bytes of data to be exchanged [1]. This calls for higher data rates, larger network capacity,higher spectral efficiency, higher energy efficiency, and better mobility [4]. Therefore, researchers have proposed the 5Gnetworks to handle the above mentioned issues resulted from billions of wireless devices. A combination of well-known and efficient technologies will be deployed in 5G networkssuch as the device-to-device (D2D) communication, the ultradense networks (UDNs), the spectrum sharing, the centimeterwave (cmWave) or millimeter wave (mmWave), the internet ofthings (IoT), and the massive multiple-input multiple-output(MIMO) [5][6].

MIMO is a key technology that has been used since the thirdgeneration (3G) wireless networks to enhance performance ofthe wireless transceivers [7]. The idea is to use multiple antennas in the transmitter and the receiver to increase the spectralefficiency, the range and/or the link reliability. However, due tomultiple interfering messages being transmitted from different antennas, the MIMO receiver is expected to use a detectionmechanism to separate the symbols which are corrupted byinterference and noise. The MIMO detector has been a topic ofgreat interest during the past 50 years. Massive MIMO systems [8], [9] with a large number of antennas (up to hundreds) atthe base station (BS) or access point are a natural extension ofthe conventional small-scale MIMO technology. The massive MIMO base station can serve a large number of user terminals witha single or few antennas in the same frequency band. Thekey feature of the classical massive MIMO system operatingbelow 6 GHz carrier frequency is that the number of BSantennas is clearly larger than the total number of antennas inthe user equipment within the cell or service area. Thereby themultiuser interference averages out to appear just as increasedadditive noise with the problems in channel estimation due tothe pilot contamination [10].The classical massive MIMO technology has been adoptedfor the fifth generation (5G) communication systems for below6 GHz, wherein the scattering and multipath propagation inradio channels is rich. Thereby the interference averagingdue to the large number of antenna elements makes theconventional Matched Filter (MF) based receivers often approximately optimal. Very large antenna arrays are also needed athigher carrier frequencies, i.e., cmWave or mmWave bands andbeyond toward the THz band. However, propagation channelsare therein much more directive making the interference conditions rather different. Therefore, the term massive MIMO hasnot classically been used for those communications concepts,but this terminology varies from paper to paper. Large arraysare easier to implement and pack in the higher frequenciesdue to the smaller size of antennas. Therefore, the massiveMIMO detection techniques may have a role in the cmWaveor mmWave systems, although the propagation characteristicsof the channels make the multiuser interference scenario quite different. We focus on the classical massive MIMO notion anddetectors for systems operating below 6 GHz carrier frequency in this survey.

Outline: The remainder of this paper is organized as follows.

Section II briefly introduces the system model and motivation. Section III describes the proposed recursive conjugate gradient method for a massive MIMO system. Section IV shows the symbol-error-rate simulation results and comparisons. Section V presents the proposed VLSI architecture. Section VI shows the hardware implementation results and their comparisons with state-of-the-art designs. Conclusions are drawn in section VII.

2. Literature review

Kim et al. (2013), Highlight (2014), Bogale et al. (2015), Ying et al. (2015), and Noh et al. (2016) demonstrated that hybrid beamforming concepts, which are a mixture of digital and analogue beam-forming, are widely applied to massive MIMO systems. The digital beamforming portion creates base-band signals, whereas the analogue beamforming portion addresses RF chain effects by reducing the number of ADCs/DACs, which improves the outputs of power amplifiers or changes the architecture of the mixers and hence provides cost savings.Different types of hybrid beamforming systems have been designed and suggested by many researchers.

Hur et al. (2013) designed a hybrid beam-former and compared hybrid and digital beamforming in the case of downlink multiuser massive MIMO systems. They investigated the relationship between both digital and hybrid beamforming statistically by varying such factors as the RF chain parameters (ADCs and the number of multiplexed symbols). Simulation results showed that for a certain number of RF chains and ADCs, the difference in performance between digital and hybrid beamforming can be improved by reducing the number of multiplexed symbols. Furthermore, for a particular number of multiplexed symbols, increasing the number of RF chains and ADCs will increase the sum rate of hybrid beamforming that can be obtained. Recently, researchers have concentrated on de-signing and developing hybrid beamforming that can operate in mm-wave bands for massive MIMO systems.

Chen (2015), Dai et al. (2015a; 2015b), and Ghauch et al. (2016) designed hybrid mm-wave precoding for multiple objectives, such as reducing the weighted sum of squared residuals between the optimal digital beamforming design and hybrid beamforming design. Dai et al. (2015a; 2015b) ad-dressed the problem of channel estimation and hybrid precoding/detectors, and Chen (2015) and Ghauch et al. (2016) reduced the complexity of hybrid beamforming.

3. Methodology of the work

3.1 System architecture

This project mainly deals with the improvement of quality of signal for 5G communication. Even MIMO systems are playing very important role for today's technology for the improvement of reliability. Hence this project is suitable for the development of proper communication and service.

This project mainly implemented a novel architecture for the improvement of communication based the transmission of data. The second implementation is for the error detection and correction of the data for the efficient data transmission. The third part of this project is mainly focused on the implementation of synthesis results and generated power, area, timing reports. Finally comparison had done the existing methods and shown better performance of the present design.

In this section, VLSI architecture is designed to achievemassive MIMO detection based on a modified MMSE signaldetection algorithm. The architecture was designed for a casestudy of a 64-QAM, 1288 massive MIMO system. Fig. 6shows the top-level block diagram of the proposed VLSI architecture. To achieve high throughput with limited hardwareresources, the top-level architecture is fully pipelined. The VLSIarchitecture is divided into three main modules.

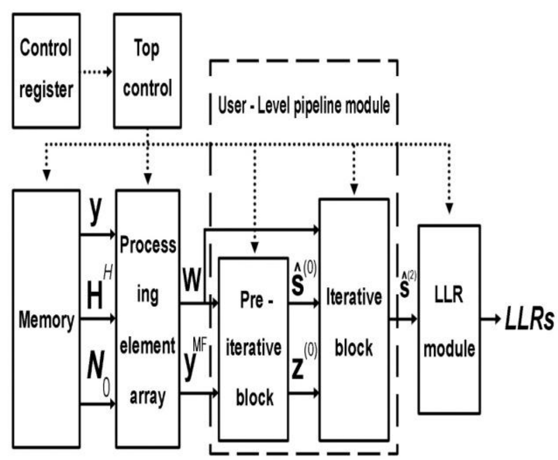

Figure 2: system architecture

4. SYNTHESIS AND SIMULATION RESULTS

For fair comparison, the same style of coding using Xilinx 14.7 ISE tool and Verilog HDL coding will be adopted to design MIMO system and presented multipliers, 8 adders and 8 subtracters. More over all of these designs will be synthesized by Synopsys Design Compiler in the same SAED 45 nm CMOS technology for obtaining area of core, power and timing for distinctive size of word. The properties of physical synthesis analysis are compromised with maximum combinational gate delay, consumption of area, area of core, ADP, PDP are represented in Table 1. The results in table 1will alter with the adopted coding style of HDL and the available options of optimization in synopsis tool.

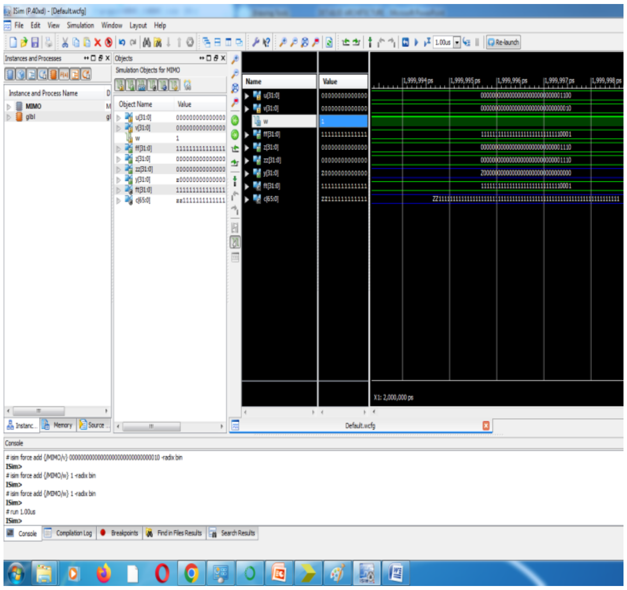

Figure. 3: Simulation Result of MIMO system

Above Fig. 2 shows the simulation result of High Speed MIMO system 32 bit length input sequence is taken for the implementation of the described High Speed and Low Power MIMO system and it is clear that described method acquires less power, less area and less delay which automatically increases the speed. ADP and PDP plots are represented for 32 bit input sequence in Fig. 3 and Fig. 4 respectively. RTL View of 32-Bit MIMOis shown in below Fig. 3.

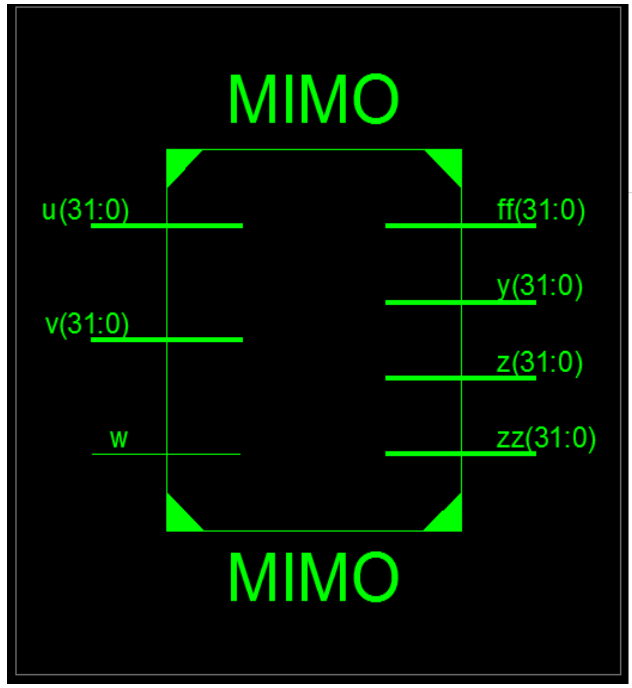

Fig. 4: RTL View of 32-Bit HC binary adder

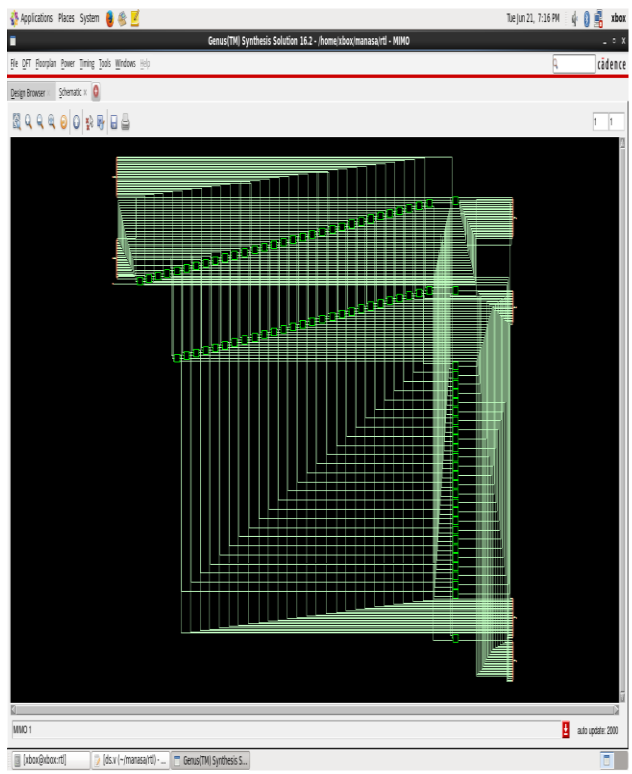

Fig. 4: Synthesis Layout

5. comparisons

Name of the Module	Power (μw)	Area (μm^2)	Timing
BEAMFORMING MIMO	22465730	39381	737(
CURRENT MIMO	1325974.030 (NW)	2010 (NM)	5350 (:

Conclusion

We have proposed a modified massive MIMO detection algorithm architecture based on the development of VLSI architecture. In addition, according to the properties of massive MIMO systems, a quadrant-certain-based initial method is proposed. Moreover, an approximated VLSI structure computation method is designed and proposed. The simulation results are carried out from Xilinx 14.3 and synthesis results are extracted from Cadence Genus tool using 90nm technology.

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