DESIGN AND DEVELOPMENT OF SWITCHED CAPACITOR MULTILEVEL INVERTER WITH SPWM TECHNQUIE

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ABSTRACT: Since fossil fuels have been depleting at an alarming rate, renewable energy has been on the rise in recent decades. However, the DC currents that will power our homes and businesses from these sources are still decades away. The vast majority of uses need for an AC connection. The process of changing direct current to alternating current has arrived. There is the usage of an inverter, a circuit that changes DC power into AC power. The inverter's efficiency is negatively impacted by the high total harmonic distortion % caused by the inverter's output harmonics. Multiple DC voltage levels may be generated using a Multi-Level inverter, which can also be employed in high-power and high-voltage applications. With lower harmonic distortion, this produces decent value output. A switched-capacitor frontend and an H-Bridge backend are provided for a cascaded capacitor-switched multilevel inverter that makes use of the SPWM approach in this research. With the frontend, voltage may be switched between series and parallel at a greater range of values than before. Increasing voltage levels is an effective way to reduce harmonic distortion. In contrast to traditional multicarrier modulation, the suggested symmetrical triangular waveform modulation may be implemented directly in analog and has a low modulation frequency. All aspects of the network architecture, including the routing protocol, the parameters used in it, the symmetry of the modulation, the Fourier analysis of data, the frequency of network operations, and the efficiency of the topology, are examined. The simulation results are then compared to those obtained in an experiment with a rated output frequency of 25 kHz. In addition, a low-power prototype model has been produced.

Key Words: Pulse Width Modulation, Cascaded Multilevel Inverter, Switched Capacitor

I.INTRODUCTION

Renewable energies play a crucial role in meeting our energy needs. More and more people are starting to realize the need of using renewable energy sources like wind and solar to power their homes and businesses. So, when compared to conventional production systems that rely on fossil fuels, the stated energy resources are seen as a legitimate alternative for producing electricity. To alleviate the energy issue, RESs are used alongside conventional power plants.

With the help of an inverter, DC electricity may be transformed into AC power and used to power a wide variety of electronic devices. Many modern industrial processes call for the use of high voltage and MW power, as do certain utility tasks and motor drives. It is not simple to immediately connect a single power semiconductor switch in a medium voltage grid. The MLI structure therefore emerges as a viable alternative in both high-power and medium-voltage settings.

A multilayer inverter provides a number of benefits in one, such as the ability to use renewable energy sources and high power ratings. When working with higher-powered equipment Renewable energy sources, such as fuel cells, solar cells, and wind turbines, may be readily interfaced with multilevel inverters. It is probable to employ power semiconductor switches coupled in series with a number of lower voltage dc sources that forms a staircase waveform in order to attain high power. Batteries and capacitors, as well as other forms of renewable energy, may be utilized to create a system that can provide power from numerous

eISSN 1303-5150

voltages. Efforts to boost voltage have been the subject of several investigations. Increasing the voltage levels effectively using switched capacitor multilevel inverter circuitry requires a complicated control method. Because of the way the components of a 1-to-5 pulse width modulated inverter are arranged, the maximum voltage that can be generated by the circuit is just a few volts. The given switched capacitor multilevel inverter has a Full-bridge Cell as its output and a switched capacitor cell (SC cell) as its input. A switching capacitor H-bridge multilevel inverter with a single power supply is proposed here. A single dc source is presented in this study to replace the current setup of several, independently operating dc sources using a switched capacitor. The benefits of the proposed work include: 1. Capability to maintain one's own equilibrium. The amount of leakage current is reduced. 3)An insignificantly high THD. Increases alternating current voltage levels.

II. PROPOSED SYSTEM

Fig.1 shows a schematic of the 9-Level Inverter's layout. Stage A comprises of SC(S1-S2) and Stage B consists of a H Bridge cell, each of which plays a unique function in the proposed inverter's workings. By using a Stage A SC(S1-S2) to configure and build the required n-levels (9 in the suggested design), and a Stage B H Bridge to reverse the polarity of the inverters, we may achieve this. The n-level AC output from Stage A's SC(S1-S2) DC output may be used in a number of contexts. There are two direct connections between Stage A SC (S1 and S2) and connected to the DC power source.

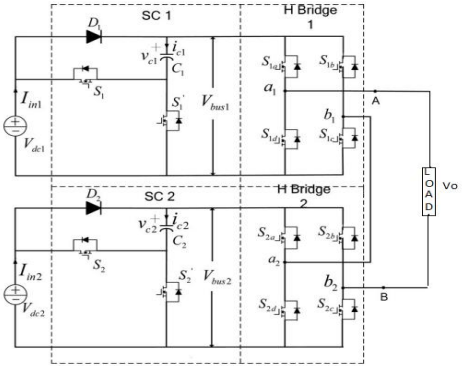

Figure. 1. 9-level SC based ML inverter with reduced switches.

There are nine distinct operating modes for switch configurations, numbered from zero to eight. Stage B may be broken down into two basic conditions: the first is reached when switches S1a, S1b, S2a, and S2b are all set to "1," and the second is reached when switches S1c, S1d, S2c, and S2d are all set to "0." This is how mode 0 is implemented. Capacitors C1 and C2 are charged to Vin when the output voltage is zero and switches S1c, S1d, S2c, and S2d are logically conditioned ON "1." This is the second requirement for mode 0. Bus 1 and Bus 2 both have voltages of Vin. Mode1 is reached by closing switches S1', S2' in Stage A and S1a, S1b, S2a, and S2c in Stage B, and is one of the five fundamental building operations of the 9-Level inverter. Switches S1', S2' in Stage A and S1a, S1b, S2a, and S2c in Stage B are conditioned "1" or closed, charging capacitors C1, C2. Vo = Vin follows from this calculation.

To enter Mode 2, shut the Stage A switches S1' and S2' and the Stage B switches S1a, S1c, S2a, and S2c. Switches S1', S2' in Stage A and S1a, S1c, S2a in Stage B ensure that capacitors C1 and C2 are kept charged. In the second stage B, all S2c are closed, or conditioned to the value 1. Vo = 2Vin is the logical conclusion of this process.

Switches S1',S2 in Stage A and S1a, S1c, S2a, and S2c in Stage B must be closed to enter Mode 3. The condition "1" (or closed) is applied to switches S1',S2 in Stage A and S1a, S1c, S2a, S2c in Stage B. The second capacitor, C2, begins to leak. For this reason, we get Vo = 3Vin as an answer.

Closed switches S1, S2 in Stage A and S1a, S1c, S2a, S2c in Stage B produce Mode 4. When switches S1, S2 in Stage A and S1a, S1c, S2a, S2c in Stage B are conditioned "1" or closed, the capacitors C1, C2 begin discharging. The calculation concludes that 4Vo is equivalent to 2Vin.

In Stage A, closing switches S1' and S2' puts the system into Mode 5, whereas in Stage B, closing switches S1c, S1d, S2b, and S2d puts the system into Mode 5. Switches S1', S2' in Stage A and S1c, S1d, S2b, and S2d in Stage B are conditioned "1" or closed, beginning the charging process for capacitors C1 and C2. Vo = -Vin is the logical conclusion of this expression.

Closed switches S1', S2' in Stage A and S1b, S1d, S2b, and S2d in Stage B produce Mode 6. Because switches S1', S2' in Stage A and S1b, S1d, S2b, and S2d in Stage B remain conditioned "1" or closed, capacitors C1 and C2 continue to be charged. That's why the answer to the equation is -2Vo minus 2Vin.

eISSN 1303-5150

Closed switches S1', S2 in Stage A and S1b, S1d, S2b, S2d in Stage B produce Mode 7. Discharge of capacitor C2 begins when switches S1', S2 in Stage A and S1b, S1d, S2b, S2d in Stage B are all conditioned "1" or closed, respectively. Vo = -3Vin is the logical conclusion of this process. If switches S1, S2 in Stage A and S1b, S1d, S2b, and S2d in Stage B are closed, then Mode 9 is activated. Since switches S1, S2 in Stage A and S1b, S1d, S2b, and S2d in Stage B are conditioned "1" or closed, the capacitors C1 and C2 begin to discharge. This calculation leads to Vo = -4Vin as the final output.

Switching, Capacitor Logic, and Voltage Output Table1

On-state switches	Output Voltage	Capacitor State
S1a, S1c, S2a, S2c, S1, S2	4Vin	C1, C2 Discharging
S1a, S1c, S2a, S2c, S1'S2	3Vin	C2 Discharging
S1a, S1c, S2a, S2c, S1', S2'	2Vin	C1, C2 charging
S1a, S1b, S2a, S2c, S1', S2'	Vin	C1, C2 charging
S1a, S1b, S2a, S2b, S1', S2' Or S1c, S1d, S2c, S2d	0	C1, C2 charging
S1c, S1d, S2b, S2d, S1', S2'	-Vin	C1, C2 charging
S1b, S1d, S2b, S2d, S1', S2'	-2Vin	C1, C2 charging
S1b, S1d, S2b, S2d, S1', S2	-3Vin	C2 Discharging
S1b, S1d, S2b, S2d, S1, S2	-4Vin	C1, C2 Discharging

III. MULTI-CARRIER SPWM CONTROL TECHNQUIE

For a multilayer inverter, multi-carrier SPWM is the most reliable method of control. whereby several triangular waveforms on different carriers are used to complement a single sine wave. If there are n levels, then n minus one carrier signals are needed to produce a gate pulse. When a carrier signal of frequency fc is compared to a reference signal, such as a sinusoidal waveform, pulses may be produced. A sine reference signal is used to evaluate each carrier. When a carrier wave's amplitude is smaller than that of a sinusoidal reference wave, a switch is thrown. The switching frequency of Stage B converter and the harmonics in the output of multilayer converter are both determined by the carrier signal frequency. The fundamental frequency is determined by a reference wave's frequency. The modulation index changes depending on the strength of the reference signal. As can be seen in fig.2, the amplitude of the reference signal, Ar, is either less than or equal to that of the triangle signals, Ac. This method is effective in decreasing both distortion and the lowest order harmonics (LOH).

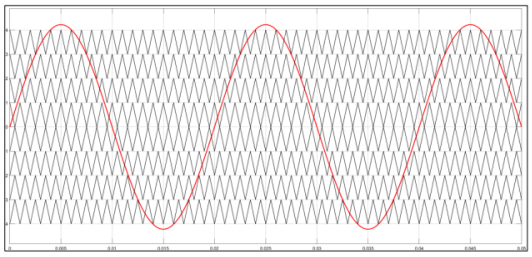

Figure.2 The comparison between sine signal and triangle signals

IV.SIMULATION& HARDWARE RESULTS

A) SIMULATION

In Figure.3 we can see the MATLAB/SIMULINK Model of MC SPWM, and in Figure.4 we can see the control block of MC SPWM in action.

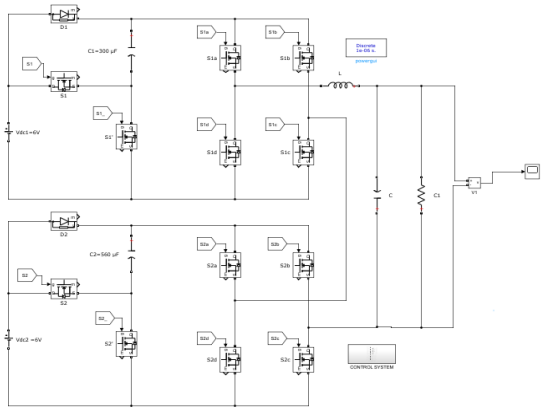

Figure.3 MATLAB/SIMULINK circuit diagram of MC SPWM

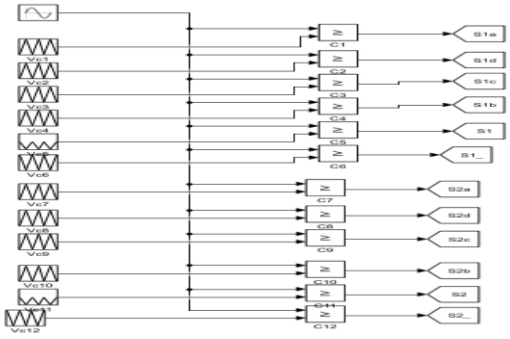

Figure.4 Control system of PSM

In the multi-carrier PWM block shown in Fig. 4, for example, a comparison is made between a number of carrier waves and a single sinusoidal waveform to determine the timing of the gate pulses that turn the Switches on and off. The carrier wave amplitudes are as follows: The voltages 1V, 2V, 3V, 4V, 5V, 6V, 7V, 8V, 9V,

eISSN 1303-5150

10V, 11V, and 12V are represented by 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 volts, respectively.
The standard Sinusoidal reference signal has an 8V amplifier.
The suggested converter has been simulated in the MATLAB Simulink environment. Each of the following factors is taken into account. For this example, we'll assume that the forward voltage drop and internal on state resistance of diodes D1 and D2 are 0.6V and 50m, respectively, and that the value of the load resistance is R 0 = 50, and that the capacitor value of module 1 is C1 =300 F and that the capacitor value of module 2 is C2 =560 F. f s, the signal's output frequency, is 25 kilohertz.

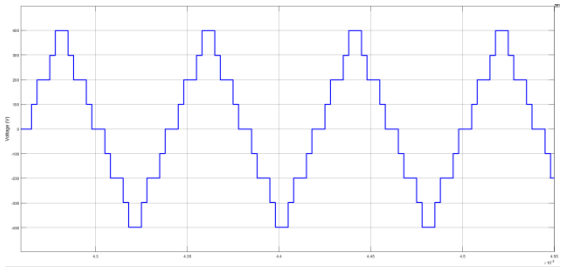

Figure.5 Output voltage

B) HARDWARE IMPLEMENTATION

The inverter's maximum power output is 40W. The inverter can produce up to 24 volts of output power at its peak. We can utilize lamps or tiny motors with this amount of electricity. It's a working model of the project that's currently under development.

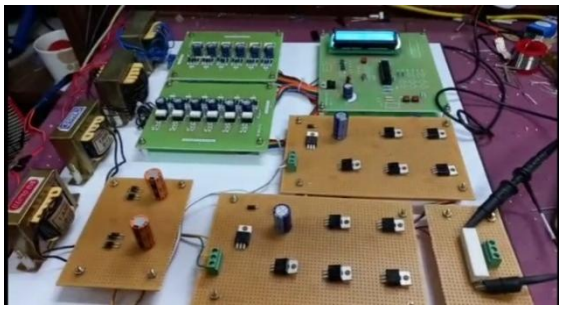

Figure.6Hardware model of switched capacitor based 9-level Inverter

From the DC supply, there are nine different voltage levels (Vdc, 2Vdc, 3Vdc, 4Vdc). Only two sources are utilized in this setup. Consequently, we refer to this set-up technique as an asymmetrical multilevel inverter. Both the modulation index and the DC voltage delivered to the inverter determine its output. The inverter's voltage levels may be expanded by experimenting with various settings. To provide the inverter circuit with PWM signals, an ADSPIC controller is employed. This single-phase inverter uses MOSFET switches (IRF840).

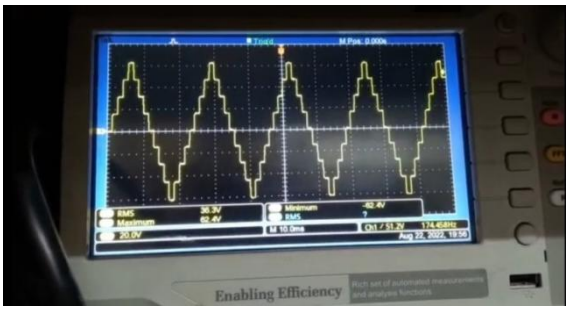

Figure.8Voltage Waveform Observed in the CRO

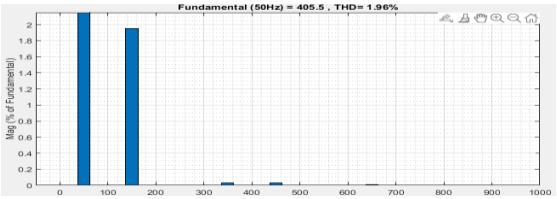

Figure.9 THD% of Output voltage

CONCLUSION

The research presents a unique cascaded multilevel inverter based on a switched-mode power supply (SC). The topology of the nine-level circuit is analyzed thoroughly. The number of switching devices in the proposed inverter may be drastically reduced in comparison to a traditional cascaded multilevel inverter. Using the PSM and SPWM approach, a 9-level cascaded H-bridge MLI has been designed and constructed. As it leaves from, the SPWM method generates lesser THD than PSM.

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