Design of 16x16 Vedic multiplier for fast DCT computation using 45nm Technology

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Abstract

Digitizing a natural image or conversion from time domain to frequency domain require transformation of the analog data. Discrete Cosine Transform is one of the many methods available for transformation. DCT is extensively computational with many multiplier and adder units. Its known fact that multiplier block consumes more power and for battery powered portable devices an alternative algorithm is to be used which supports low power vlsi. And if we look back to our ancient heritage of math's, Vedic mathematics becomes a boon to design DCT. Computational steps are reduced in Vedic multiplier. A comparative study is done between 16x16Vedic multiplier and Booth multiplier which are implemented using ISE design suite 14.7with area and power report generated cadence 45nm technology.

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Introduction

Low power methods can be applied at different levels of design steps. At system level specification the power consumed at different blocks are estimated, dynamic power is considered at algorithm level and short circuit leakage current is considered at circuit level.The strategies followed for low power VLSI are as shown below.[7]

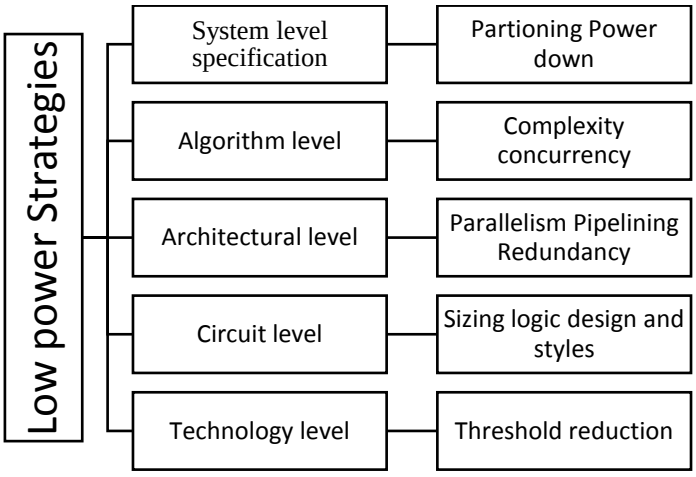

Fig1: Low Power Strategies.

With this brief introduction of low power strategies, the next part of the paper includes matrix representation of DCT coefficients, literature review about Vedic multiplier its line diagram, schematic symbol, the design of 16x16 Vedic multiplier using 2x2, 4x4 and 8x8 multiplier. The gate count report and the power analysis report are shown in the result and discussion section.

DCT is a computationally intensive operation and many methods are followed to implement DCT. Since multiplication is the main computation operation in DCT, design of the multiplier is main aim of this research paper. Multiplier design is the significant step in DCT computation.

The strategy adopted in this paper is at algorithm level to design a vedic multiplier. One of the basic computational unit in DCT is matrix multiplication and 2-D DCT equation is given below where the image p(x,y) is multiplied with cosine values as in equation 1. Since DCT is included by JPEG for transformation in standard image compression method the value of N=8 can be taken for 8x8 matrix as in equation 2

$$D(i,j) = \frac{1}{\sqrt{2N}} C(i)C(j) \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} p(x,y) \cos\left[\frac{(2x+1)i\pi}{2N}\right] \cos\left[\frac{(2y+1)j\pi}{2N}\right]$$

$$C(u) = \begin{cases} \frac{1}{\sqrt{2}} & \text{if } u = 0 \\ 1 & \text{if } u > 0 \end{cases} \qquad \text{.....(1)}$$

$$D(i,j) = \frac{1}{4} C(i)C(j) \sum_{x=0}^{7} \sum_{y=0}^{7} p(x,y) \cos\left[\frac{(2x+1)i\pi}{16}\right] \cos\left[\frac{(2y+1)j\pi}{16}\right] \qquad \text{.....(2)}$$

$$T_{i,j} = \begin{cases} \frac{1}{\sqrt{N}} & \text{if } i = 0 \\ \sqrt{\frac{2}{N}} \cos\left[\frac{(2j+1)i\pi}{2N}\right] & \text{if } i > 0 \end{cases}$$

The coefficients of DCT multiplied with pixel values of first column of the image is as shown below for 8x8 matrix. [2]

$$\begin{bmatrix} Y(0) \\ Y(1) \\ Y(2) \\ Y(3) \\ Y(4) \\ Y(5) \\ Y(6) \\ Y(7) \end{bmatrix} = \sqrt{\frac{1}{4}} \begin{bmatrix} C_4 & C_4 & C_4 & C_4 & C_4 & C_4 & C_4 & C_4 \\ C_1 & C_3 & C_5 & C_7 & -C_7 & -C_5 & -C_3 & -C_1 \\ C_2 & C_6 & -C_6 & -C_2 & -C_2 & -C_6 & C_6 & C_2 \\ C_3 & -C_7 & -C_1 & -C_5 & -C_5 & C_1 & C_7 & -C_3 \\ C_4 & -C_4 & -C_4 & C_4 & C_4 & -C_4 & -C_4 & C_4 \\ C_5 & -C_1 & C_7 & C_3 & -C_3 & -C_7 & C_1 & -C_5 \\ C_6 & -C_2 & C_2 & -C_6 & -C_6 & C_2 & -C_2 & C_6 \\ C_7 & -C_5 & C_3 & -C_1 & C_1 & -C_3 & -C_5 & -C_7 \end{bmatrix} * \begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} \qquad \text{.....(3)}$$

The entire image should be multiplied with DCT coefficients, therefore multiplier plays a important role in DCT computation.

Literature Review

Multiplier design was very important unit in computing DCT and consumption of power was huge so design of low power multiplier and the alternatives for it became the aim of research work. At this juncture the unique and dedicated contributions of Sri Bharati Krishna Thiraji Maharaj in the field of vedic mathematics is a boon for VLSI designers. From the year 1911 to 1918Swamiji made an attempt to bring the sutras of vedic mathematics together and as result of his research in this field vedic mathematics text book was published in 1965. [1]

UrdhvaTiryakbhyam (UT)sutra reduces the computational complexity in DCT. Since area

power consumed and speed are the main constraints in low power design vedic multiplier is a solution for the design. [10-12]
Methods like sub-expression reduction, canonical signed representation, Binary DCT and INT dct are used for low power design at architectural level discussed by the authors in the papers[8-9].
A new method known as algebraic integer involves representing the real cosine values where they are mapped to array of integers and then approximated using fixed point representation.
Arai algorithm is also used for designing DCT hardware architecture by using AI coefficient for row and column. For decoding the integers into fixed format final reconstruction step is used .adders and shifters are replacing multipliers reducing size of memory are the different ways in designing low power VLSI circuits.[5-6] .

Design of 16x16 vedic multiplier using 2x2,4x4 and 8x8 multiplier

2x2 vedic multiplier

In multiplier unit partial products are obtained using AND gates and adders are used to add the products obtained. Vedic multiplier uses the concept of parallel computing equivalent to human brain functioning. Parallel computing saves power and area and supports low power VLSI design.

Vedic mathematics is a gift of ancient Indian heritage where the complexity of computation is decreased.16x16 bit multiplier is designed using 2x2, 4x4 and 8x8 bit vedic multiplier. UrdhvaTiryakbhyam UT is used for fast multiplication operations, the latency in generating partial products is reduced by this method. Since it uses parallel computing for partial products. The sutra stands for vertical and cross. Multiplication of two bit inputs ranging from a[1:0], b[1:0] is shown in the figure. It includes vertical wise multiplication and crosswise multiplication as we usually multiply in our brain.

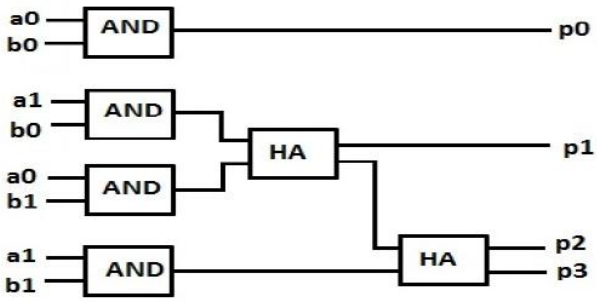

Fig 2: Schematic diagram of 2x2 Vedic Multiplier

16x16 Vedic multiplier

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Similarly 4x4 and 8x8 bit multiplier can be designed using 2-bit multiplier. The block diagram for 16x16 multiplier is shown below, consisting of 8x8 Vedic multiplier and 16-bit ripple carry adder.

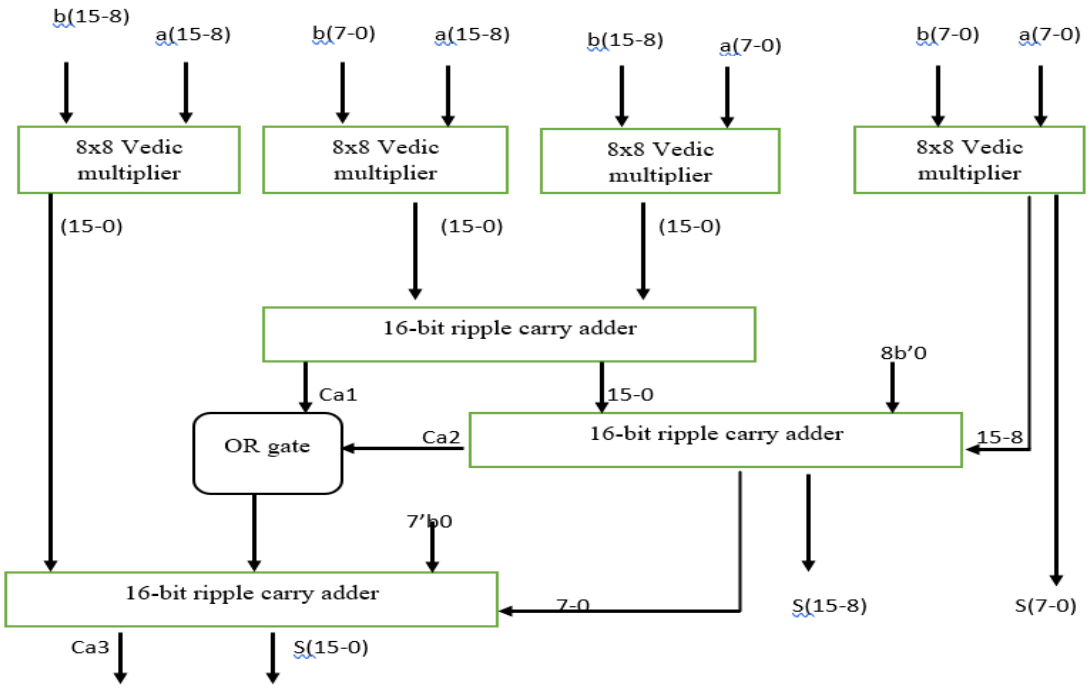

Fig 3: Block Diagram of 16x16 Vedic Multiplier

Results and Discussion:

Verilog code is written for 2x2,8x8,16x16 Vedic multiplier and cadence virtuoso tool was used to generate power and delay report.

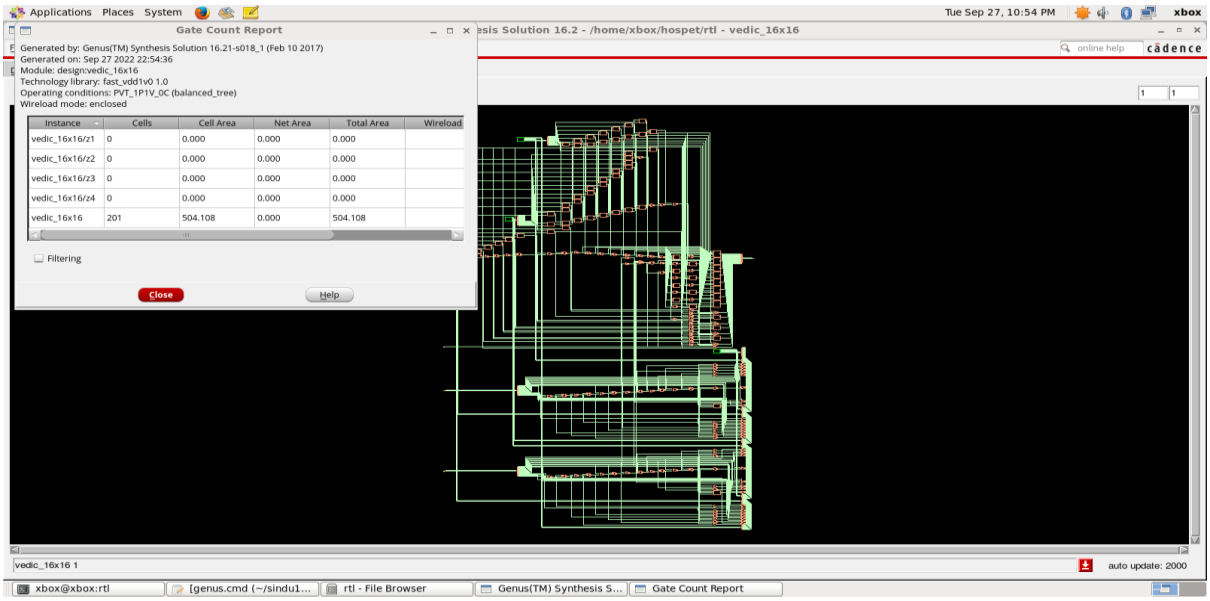

Fig 4 Gate Count Report of Vedic Multiplier

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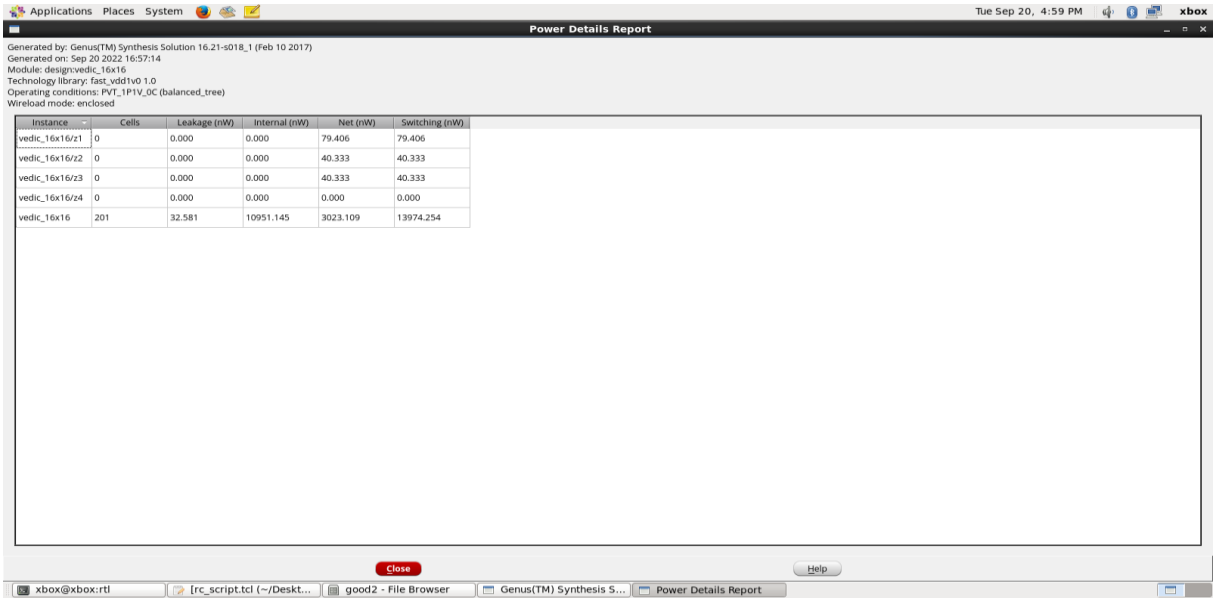

Fig 5: Power Report of 16x16 Vedic Multiplier

Comparative study of Vedic multiplier and booth multiplier is done in below table. The important performance parameters like power, speed and area are compared.

Table 1:Comparison of both the multipliers

Multiplier	Cells	Power(nW)	Area(μm^2)
Vedic	201	3023.109	504.108
Booth	1239	472638.281	13264.672

The performance of Vedic multiplier in terms of power area and timing is better than booth multiplier and these features support low power design.

Conclusion

Approach of Vedic multiplier is very similar to computation in human brain. Parallel computing reduces the heat dissipation and delay. The cells count is also reduced which in turn reduces area. Vedic multiplier can be a good alternative for booth multiplier and design of processor using Vedic multiplier will be a solution for less power consumption in battery powered portable devices. The sutras in Vedic mathematics have many possibilities and intensive research work is needed so that multiplier and divider are designed for low power.

References

1. Jagadguru Swami Sri Bharati KrisnaTirthaji Maharaja, *VedicMathematics: Sixteen Simple Mathematical Formulae from the Veda*,Delhi (1965).
2. Anil .K. Jain,"Fundamentals Of Digital Image Processing ",Prentice-Hall, Inc, 1989.
3. N. Ahmed, T. Natarajan, and K. R. Rao, "Discrete Cosine Transform",*IEEE Trans. Computers*, 90-93, Jan 1974.
4. Rafael C. Gonzalez, Richard Woods, Steven L. Eddins," Digital

imageprocessing using Matlab", Prentice Hall,2003.

5. Gary J Sullivan, and Jens-Rainer Ohm, and Woo-Jin Han, and ThomasWiegand, "Overview of the high efficiency video coding (HEVC)standard, " IEEE Transactions on circuits and systems for videotechnology, vol. 22, no. 12, pp. 1649-1668, 2012.
6. Arjuna Madanayake, and Renato J Cintra, and Denis Onen, and VassilS Dimitrov, and NilankaRajapaksha, and Leonard T Bruton, and AmilaEdirisuriya, "A row-parallel 8_ 8 2-D DCT architecture using algebraicinteger-based exact computation, " IEEE transactions on circuits andsystems for video technology, vol. 22, no. 6, pp. 915-929, 2012.
7. Douglas A.Pucknell and Kamran Eshraghian (2001), ' Basic VLSI Design' Prentice Hall of India private Ltd., New Delhi, pp. 240-253.
8. Maher Jridi,1 Ayman Alfalou, and Pramod Kumar Meherx "Optimized Architecture Using a Novel Subexpression Elimination on Loeffler Algorithm for DCT-Based Image Compression" 2012Hindawi Publishing Corporation VLSI Design
9. Design and Implementation of 2D-DCT by Using Arai Algorithm for Image CompressionPratiksha R. KumbhareM.Gokhale Journal of Advance Research in Electrical & Electronics Engineering 2015
10. NuriddinSafoev and Jun-Cheol Jeon , "Design and Evaluation of Cell Interaction Based VedicMultiplier Using Quantum-Dot Cellular Automata" 23 June 2020
11. Hardware Efficient Architecture for 2D DCT andIDCT using Taylor-series Expansion ofTrigonometric FunctionsDebasish Mukherjee, Student Member, IEEE, and Susanta Mukhopadhyay 2019
12. Design of Discrete Cosine Transform using Vedic MathematicsDr.S.Kirubakaran, Mr.K.Saravanan, Dr N.Rajeshkumar 2020
13. Implementation of Vedic Multiplier in ImageCompression using DCT AlgorithmS. S. Kerur, Prakash Narchi, Harish M Kittur, Girish V. A 2014
14. *Suryasnata Tripathy, L B Omprakash, Sushanta K. Mandal, B S Patro, "Low power multiplier architectures using vedic mathematics in 45nmtechnology for high speed computing" 2015
15. Applications of Vedic multiplier - A ReviewRashiKhubnani, Tarunika Sharma, Chitirala Subramanyam 2021
16.

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