Modeling and Analysis of High RF Behavior of Nano Scale Surrounding Gate MOSFET

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Abstract

This paper presents novel modeling of nano-scale Surrounding Gate MOSFET operating in sub-threshold region. The current is obtained using surface potential and varying device parameter like gate - source voltage and drain - source voltage. The channel Length L was 40nm for proposed SG MOSFET. In continuation of work the Drain Induced Barrier Lowering (DIBL) of SG MOSFET also modeled and analyzed .The transconductance of the proposed device modeled and analyzed for various values of drain voltages. The drain conductance and channel length modulation of the device modeled for various values of drain to source voltages of proposed device.

Keywords —Surrounding Gate MOSFET, DIBL, Channel length modulation, Surface potential.

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I. INTRODUCTION

The surrounding gate MOSFET (SG MOSFET) is the most promising solution to the limitation of scaling and increment in device performance. In SG MOSFET, gate, drain and source are organized vertically and pillar's sidewalls used as the channel region as shown in the Fig. 1. Another salient feature of SG MOSFET is that the width and length of the channel are depend on the pillar height and parameters. [1]. So the channel length may be shrinked without modifying the transistor's utilized area ensuing huge packing density [2, 3].

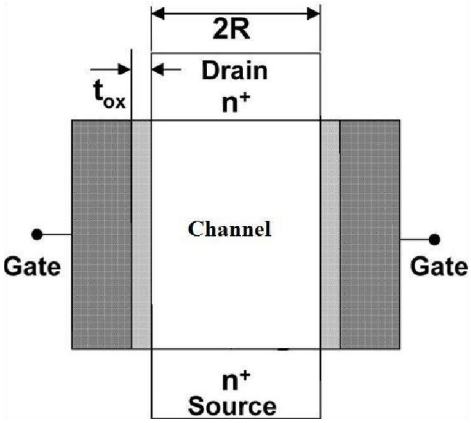

Fig. 1 Cross- sectional cut view of Surrounding Gate MOSFET

In addition to the above feature, SG MOSFET also give other characteristics such as higher current drive, small substrate bias effects, steep sub threshold characteristics, high reliability and increased short channel immunity [1, 4]. It was further explored that use of cylindrical/surrounded architecture results in scaling down of CMOS inverter's occupying area by 50% as compared to bulk MOSFET [1]. Comprehensive research has been carried out on SG MOSFET in terms of analytical modeling [5, 6] numerical analysis [7], quantitative description of channel length, simulation and device fabrication [8].

In this paper, the Single Material Gate (SMG) SG MOSFET architecture has been proposed extensively, and an analytical model to study about current - voltage characteristics and the analysis to obtain the small signal parameters such as drain conductance and transconductance. As the dimensions of the device reduces, the short channel effects (SCEs) such as drain induce barrier lowering and channel length modulation strongly affect the conduction mechanisms. However, no analytical model is available for single material gate engineered SG MOSFET which takes into account the effect of above short channel effects. The study demonstrated that Short channel effects are efficiently suppressed through SG MOSFET design, which results in a rise in transconductance and decrease in drain conductance [9, 10].

II. DEVICE STRUCTURE - PARAMETERS

The structure of Surrounding Gate MOSFET is depicts in Fig. 2 for a channel length of L =40nm, radius of the device, R=15 nm, oxide thickness, t_{ox}= 3nm, doping density (N_D) is 5x10^{19} cm^{-3}, doping in substrate, with doping density (N_A) of 1x10^{16} cm^{-3} and metal gate work function (Φ_m) is 4.8 eV.

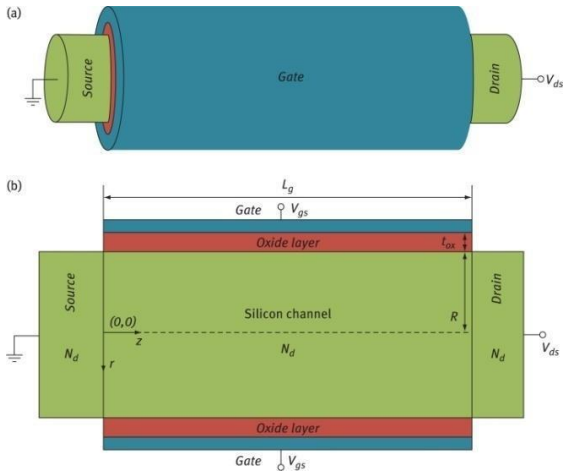

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Fig. 2 Surrounding Gate MOSFET Structure

The SG MOSFET is required less voltage as compared with planer MOSFET. SG MOSFET device performance is better than other MOS devices. SG MOSFET shows minimal leakage current and less power dissipation [10, 17]. Table 1 shows the device Parameters of Surrounding Gate MOSFET.

TABLE I Device Parameters of Surrounding Gate MOSFET

Parameters	**Values**
Boltzmann's Constant (K)	1.3807 x10^{-23} J/K
Permitivity in Vacuum (ε_o)	8.8542x10^{-12} F/m
Charge (q)	1.6021x10^{-19} C
Temperature (T)	300K
Device Thermal Voltage (V_T)	0.0258V
Energy Band Gap (E_g)	1.08eV
Electron affinity (χ)	4.17eV
Carrier concentration (Conduction band)(N_c)	2.8x$10^{19}$$cm^{-3}$
Carrier concentration (Valence band) (N_v)	1.04x$10^{19}$$cm^{-3}$
Carrier concentration of Si (Intrinsic) (n_i)	1.45x$10^{10}$$cm^{-3}$

III. ANALYTICAL MODELING

Here we obtained the various characteristics of SGMOSFET which explores the device performance in different regions. The drain current is calculated and find an expression with respect to the source and drain ends.

$$I_{ds}(z) = 2\pi R Q_n(z) \frac{\mu_n \dfrac{dV(z)}{dz}}{1 + \dfrac{1}{E_{sat}} \dfrac{dV(z)}{dz}} \quad (1)$$

2πR is width of device, where R is the device radius. V(z) is channel voltage and electric field is $\mathrm{dV(z)}/dz$ towards in z direction. E_{sat} is known as critical field =, $2V_{sat}/\mu$, saturation velocity is V_{sat} and mobility is μ.

$$\mu_n = \frac{\mu}{1 + \theta_i (V_{gs} - V_{th})} \quad (2)$$

Where,

$$\mu = \frac{\mu_0}{\sqrt{1 + \left[\dfrac{N_A}{N_{ref} + \dfrac{N_A}{S}} \right]}} \quad (3)$$

Mobility of electron is μ_0= 677cm^2/Vs. S = 350, N_{ref}= 3x10^{22} m^{-3}, N_A is doping concentration. $Q_n(z)$= Surface charge density is

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$$Q_n(z) = C_{ox}\left(V_{gs} - V_{th} - V(z)\right) \quad (4)$$

Where, Oxide capacitance – gate

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (5)$$

Putting these equations in Eq. (1) and integrate the expression, the drain current is obtained as

$$I_{ds} = \frac{2\pi R\mu C_{ox}\left(V_{gs} - V_{th} - \left(\frac{V_{ds}}{2}\right)\right)}{L\left(\frac{1}{V_{ds}} + \frac{1}{LE}\right)V_{ds}} \quad (6)$$

The expression for saturation region drain current is

$$I_{dsat} = 2\pi R V_{sat} Q_{nsat} \quad (7)$$

Where, I_{dsat} is saturation drain current, inversion charge is Q_{nsat} and V_{ds}= V_{dsat} is expressed as

$$Q_{nsat} = C_{ox}\left(V_{gs} - V_{th} - V_{dsat}\right) \quad (8)$$

Put the Q_{nsat}value in Eq. (1) from Eq. (8) is given by

$$I_{dsat} = 2\pi R V_{sat} C_{ox}\left(V_{gs} - V_{th} - V_{dsat}\right) \quad (9)$$

Now the drain saturation voltage V_{dsat} is obtained by

$$V_{dsat} = \frac{V_{gs} - V_{th}}{1 + \frac{V_{gs} - V_{th}}{LE}} \quad (10)$$

The drain current (threshold voltage V_{th} replaced by $V_{th}^{'}$) in equation (6) is given by

$$I_{ds} = \frac{2\pi R\mu C_{ox}\left(V_{gs} - V_{th}^{'} - \left(\frac{V_{ds}}{2}\right)\right)}{L\left(\frac{1}{V_{ds}} + \frac{1}{LE}\right)V_{ds}} \quad (11)$$

The saturation current replacing with L by $(L - l_d)$.Where l_d= velocity saturation length and V_{sat}= saturation velocity [7].

$$\mathrm{I_{dsat}} = \frac{2\pi \mathrm{R}\boldsymbol{\mu}\mathrm{C_{ox}}\left(\mathrm{V_{gs}} - \mathrm{V_{th}} - \frac{\mathrm{V_{dsat}}}{2}\right)}{\frac{(\mathrm{L} - l_d)}{V_{dsat}}\left[1 + \frac{\mathrm{V_{ds}}}{(L - l_d)E}\right]} \quad (12)$$

This switching behavior of the device describes by the sub-threshold region. Here, sub-threshold region especially considers for low-power applications, like switching in digital logics and memory application etc. The subthreshold current is determine by using the surface potential is given by, [11]

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$$I_{sub}=\left[\frac{2\pi R\mu_{eff}C_{ox}}{L}\left(V_t^2\right)\left[\exp\left\{\frac{V_{gs}-V_{th}}{2V_t}\right\}\left(1-\exp\left(-\frac{V_{ds}}{V_t}\right)\right)\right]\right] \quad (13)$$

The sub-threshold current variation depicts the gate/source voltage for distinct drain/source voltage from 0.5 - 1.5 V. The length of channel (L) = 40nm.

DRAIN INDUCED BARRIER LOWERING

When device dimensions shrink down, the short channel effects like DIBL come into the picture and affect the performance of the device. DIBL is a short channel effect developed due to the reduction of threshold voltage of MOSFET at large drain voltages [10].

Now here, $V_{th,}$ is the threshold voltage in linear region and $V_{th,satur}$ is the threshold voltage in saturation region. The DIBL effect incorporate with the drain current model by

$$I_{ds(DIBL)}=\frac{2\pi R\mu_{eff}C_{ox}\left[V_{gs}-V_{th}^{'}-\frac{V_{ds}}{2}\right]V_{ds}}{L\left[1+\frac{V_{ds}}{LE_{eff}}\right]} \quad (14)$$

SURFACE POTENTIAL

Fig. 5 depicts about variation in surface potential in addition with channel length for SG MOSFET and the length of channel, *L* = 40nm, V_{ds}= 0.5V, 1V and 1.5V. Even when the drain bias is raised from 0.5 to 1.5Volts, there hasn't been any detectable change in the potential for high metal gate work function region [11].

TRANSCONDUCTANCE

The transconductance, which is a significant parameter in circuit design, must be as high as possible. Transconductance is the variation in drain current with gate/source voltage while maintaining a constant drain/source voltage. This parameter measures gain of the device [12].

$$g_m=\left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=Const} \quad (15)$$

Now differentiating equation (14) with $V_{ds,}$ the drain conductance is obtained as

(16)

$$g_{m,linear}=\frac{\left(2\pi RC_{ox}V_{ds}\right)\left[\left\{\left(Y_1\right)\left(L+\frac{V_{ds}}{E_{eff}}\right)\left(\frac{\mu_{eff}}{Y_1}+Y_2\right)\right\}-\left\{\frac{V_{ds}}{2V_{sat}}\mu_{eff}Y_1\right\}\left(Y_2\right)\right]}{L\left[1+\left(\frac{V_{ds}}{L_{eff}}\right)\right]^2}$$

(16)

Where,

$$y_1=\frac{-L^2\mu^3\theta_i}{\left[\left(\mu+\mu\theta_iV_{gs}\right)L-\mu\theta_i\left(L.V_{th}\right)\right]^2} \quad (17)$$

$$Y_2 = V_{gs} - V_{th}^{'} + \frac{V_{ds}}{2} \quad (18)$$

Similarly, the saturation region transconductance is obtained by differentiating equation, we get

$$g_{m,saturation} = \left(2\pi RC_{ox}V_{sat}\right)\left[1 - LE_{eff}\left\{\frac{LE_{eff} + 2V_{th}}{\left(LE_{eff} + V_{th} - V_{gs}\right)^2}\right\}\right] \quad (19)$$

Drain conductance

Drain conductance is the variation in drain current with drain/source voltage while maintaining a constant gate/source voltage and is defined as

$$g_{d,linear} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=Const} \quad (20)$$

Now differentiating Eq. (14) with V_{ds} the linear region drain conductance is given by

$$g_{d,linear} = \frac{L\left(1+\frac{V_{ds}}{LE_{eff}}\right)\left[2\pi R\mu_{eff}C_{ox}\left(V_{gs} - V_{th}^{'} - V_{ds}\right)\right] - \frac{2\pi R\mu_{eff}C_{ox}}{E_{eff}}\left(V_{gs} - V_{th}^{'} - V_{ds}\right)}{L^2\left[1+\frac{V_{ds}}{LE_{eff}}\right]^2} \quad (21)$$

Similarly, the saturation region drain conductance is obtained by differentiating Eq. (9) with V_{ds} keeping V_{gs} constant, we get

$$g_{d,saturation} = -\left(2\pi RC_{ox}V_{sat}\right)\left[p - LE_{eff}V_{gs}\left\{\frac{-p}{q^2}\right\} + LE_{eff}\left\{\frac{p(q) - V_{th}(p)}{q^2}\right\}\right] \quad (22)$$

$$p = \frac{\partial V_{th}}{\partial V_{ds}} \quad (23)$$

$$q = LE_{eff} - V_{gs} + V_{th} \quad (24)$$

CHANNEL LENGTH MODULATION (CLM)

When V_{ds} is exceeds from V_{dsatur}, then pinch off point comes closer to source end and voltage difference $(V_{ds} - V_{dsatur})$ is reduced throughout the distance l_d. This shows a shorter length of channel than normal channel length, which causes a rise in drain current [10, 13].

Now the saturation drain current is replacing L by $(L - l_d)$ and the CLM effect [14, 15] is taken into account is given by

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$$I_{ds(DIBL)} = \frac{2\pi R\mu_{eff}C_{ox}\left[V_{gs} - V_{th}^{'} - \frac{V_{dsat}}{2}\right]V_{dsat}}{L\left[1 + \frac{V_{dsat}}{LE_{eff}}\right]} \quad (25)$$

can be represented as

$$I_{dsat} = \frac{2\pi R\mu_{eff}C_{ox}\left[V_{gs} - V_{th} - \frac{V_{dsat}}{2}\right]V_{sat}}{(L - l_d)\left[1 + \left(\frac{V_{dsat}}{(L - l_d)E_{eff}}\right)\right]} \quad (26)$$

IV. Result and Discussion

Here drain/source voltage (V_{ds}) vary from 0 to 5Volts; Figure depicts that when V_{ds} increases drain current enhances. When (V_{gs}) increases, then the charge carriers emits from source end which also increases [18-20].

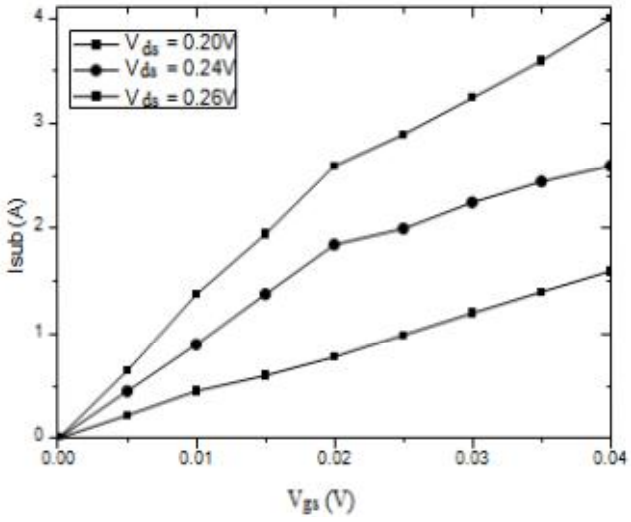

Fig. 3 Sub-threshold drain current variations at different V_{gs}

A sub-threshold current flows from source to drain in a MOSFET in the cut-off regime. In this regime, the inversion channel not created due to reason that the voltage applied at gate kept lower than threshold voltage [11, 16]. The sub-threshold current is largest when the gate voltage is close to or less than the threshold voltage and region under the gate is depleted. Fig. 3 shows that the subthreshold current enhances. Drain current rises because increase in drain voltage. Therefore, SG MOSFET design shows more gate control and hence more current.

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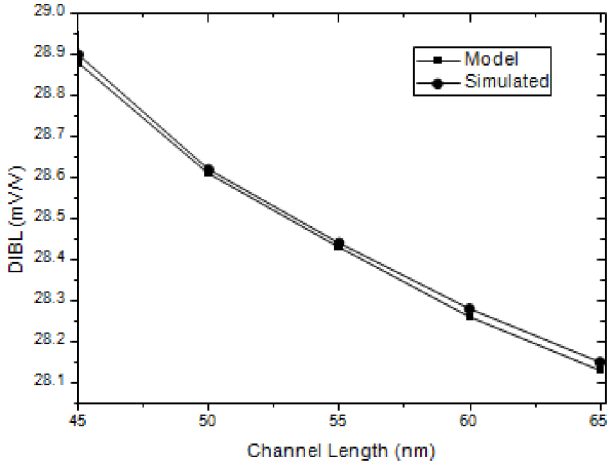

Fig. 4 DIBL variations as a Function of Channel Length

Fig. 4 depicts the changes of DIBL with the different channel lengths varying from 40 nm to 65 nm for SG MOSFET. The model is validated by the analytical results. As shown in the Fig., DIBL is much lower for SG MOSFETs, demonstrating that the SG MOSFET architecture suppresses the DIBL effect

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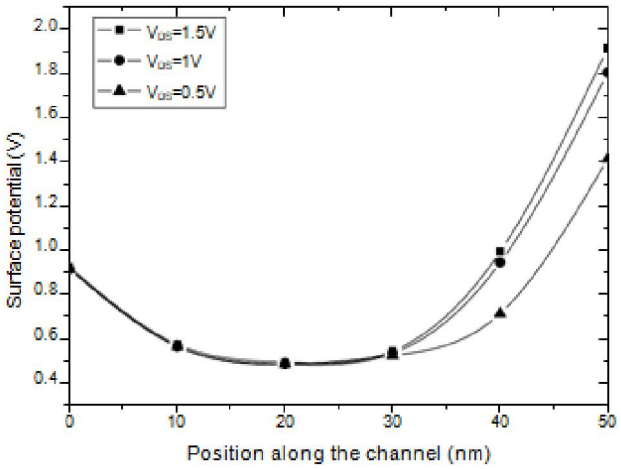

Fig. 5 Surface potential variation of SG MOSFET at different drain bias

The surface potential of SG MOSFET engineering gives reduced short channel effects depicts in Fig. 5. The position of minimum surface potential does not significantly change as the drain voltage increases. As a result, the source region is protected from drain bias variation. The drain bias increment near the drain side having low value of work-function, leads to suppression in channel length modulation

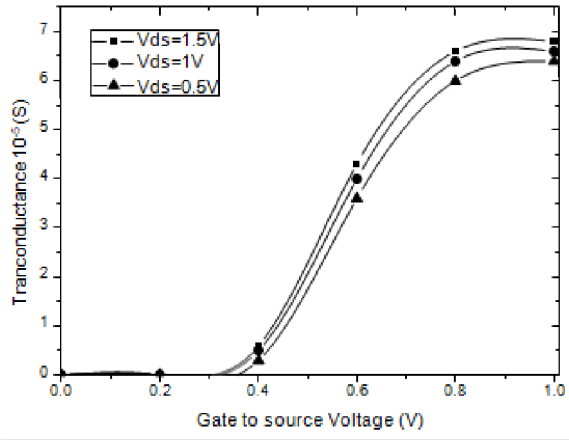

Fig. 6 Change in Transconductance at various V_{gs} for SG MOSFET

Fig. 6 depicts the transconductance variation for SG MOSFET as a factor of V_{gs} at various drain voltages, which varies from 0.5 to 1.5Volts. It is observed that SG MOSFET architecture shows the enhancement in transconductance as compared other similar devices. This is due to increase in the gate voltage higher than threshold voltage then mobile charge carriers saturates.

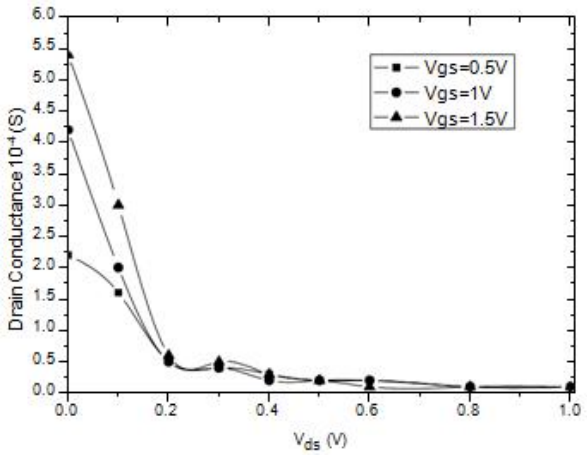

Fig. 7 Drain conductance for various gate to source voltages for SG MOSFET

Fig. 7 depicts the drain conductance variation against drain-source V_{ds} voltage at various V_{gs}= 0.5 to 1.5Volts. A good arrangement shows the simulated results. The drain conductance performance of SG MOSFET for *L*= 40nm at fixed V_{ds}=1V at various gate to source voltage from 0.5 to 1.5Volts. Drain conductance reduces with the lower values of gate voltage.

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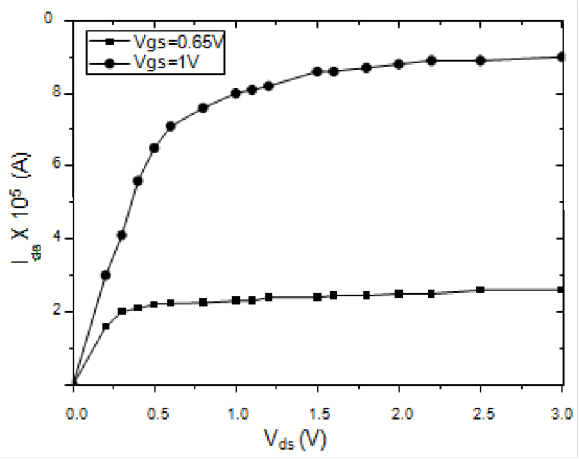

Fig. 8 Drain current variations for various gate to source voltages for SG MOSFET

The drain current can be expressed as a function of drain to source voltage is shown in Fig. 8 at V_{gs}=0.65V and V_{gs}=1V. As shown in the Fig. 8, when $V_{ds} > V_{dsatur}$, the drain current of SG MOSFET devices gradually increases. This is because when the pinch off point near to the source side, the channel length modulation effect occurs. SG MOSFET structure limits the drain control over the channel and hence it is immune to channel length modulation effect. Thus, the CLM effect is lesser in SG MOSFET structure as compared to other similar devices [21-23].

V. CONCLUSIONS

An efficient modeling presented for analyzing the high RF behavior of Surrounding Gate MOSFET. It has been observed that much better control of gate so increased current. The transconductance and drain conductance modified expression calculated. As the more doped region near the side of source a reason for reduced DIBL, which result as off state leakage current. In surface potential the suppression of short channel effect is also observed. It has been observed that improved performance of the proposed Surround Gate MOSFET in comparison to larger channel length device.

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