DESIGN AND COMPARISON OF VEDIC MULTIPLIER USING CMOS AND GDI TECHNIQUE IN 90 nm TECHNOLOGY

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Abstract

Multipliers have a great demand these days due to so many applications. Multiplier is the essential component to perform basic operation which are required in almost every circuit. Usually CMOS is used in designing of multipliers but many other techniques like GDI can be utilized to design which support low power designs. With the increasing conditions on delay, a lot of prominence is being laid on design of quick multiplications. We basically use mathematics of olden times also called vedic mathematics. They are used because they provide fast calculations and make designs uncomplicated. There are 16 sutras out of which "UrdhvaTiryagbhyam" is repeatedly used. The design of a two bit multiplier in 90m technology in cadence virtuoso has been compared with a two bit multiplier made using GDI technique. The design of fundamental components is done in the first part and then they are connected to structurevedic multiplier. The same design can be extended to high bit designs as well. There will be composite design components and many summons to face but if we use vedicmaths we can develop easy designs.[1]

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I. INTRODUCTION

The origin of a Vedic Multiplier comes from 'Vedas' which represents our ancient culture. Vedic mathematics comes from a handout composed by Swami Bharati Krishna Tirtha. It consists of various formulas related to mathematics. Multiplier is a necessary block in digital systems hence vedic multiplication algorithm is another option to implement an efficient multiplier.There are three methods to implement multiplication in Vedic mathematics. Out of three, only one method is generic method which can be applied to all cases whereas other two are for special cases. The most widely used algorithm of Vedic multiplication is UrdhvaTriyakbhyam. It can be used in all cases of multiplication. It means Vertical and Crosswise. The multiplication of two operands using Vedic multiplier is achieved by multiplication by Vertical and then going Crosswise and then adding all the results.A lot of research work over decades has led to the emergence of Vedic Multipliers as one of thefastest and low power multiplier**.** It has various advantages like partial productgeneration and additions are done togetherso there is parallel processing. It makes it more useful for binary multiplications. This in turn reduces delay, which is desired in every circuit.

The main purpose of the system was to use some techniques to solve the lengthy mathematics orally or with minimum space utilization on paper. The system of Vedic mathematics is based on 16 Sutras (Algorithms) and 13 Up-sutras(Corollaries).[2]

II. URDHVA TIRYAGHBHYAM

It is a well-known algorithm used for different cases of 0 multiplication. It reduces the number of stages required for multiplication.Suppose we have to multiply two bit numbers m1m0 with n1n0. The LSB terms are multiplied first(vertically) and then we multiply LSB of one term with higher order term crosswise and added. Here, n0 is multiplied with m1 and m0 is multiplied with n1, their product terms are then added. This is how the LSB term and term next to it are formed. In the last step we multiply the MSB of both expressions and add any carry if there from previous stage as shown.

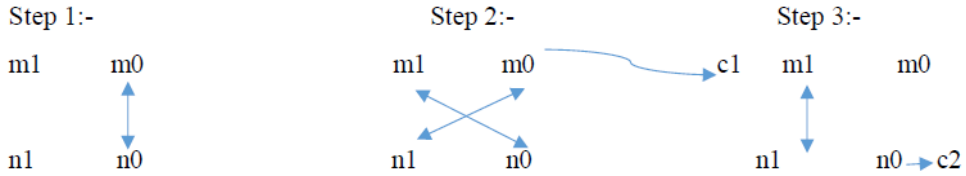

FIGURE 1: 2 BIT MULTIPLICATION USING URDHVA TIRYAGHBHYAM

III. GDI TECHNIQUE

GDI technique also called as gate diffusion input is a low power method which reduces the number of transistors used in making a design. In CMOS technology usually the number of transistors required are more as compared to this technique. It has the same design as CMOS inverter perhaps it has a different working.It consists of PMOS and NMOS as shown

G- It is regular input to gates of NMOS and PMOS

N- inputgiven to source/drain of NMOS

P- input given to source/drain of PMOS

It is easy to learn and then implement and also body of both PMOS and NMOS are joined to P or N , it can be randomly biased which cannot be done in CMOS inverter. Also, the significant difference between these methods is that in GDI P, N and G ends could be supplieda voltage like Vdd or grounded or can be given a supply of input signal as the circuit to be designed allows and hence minimizing transistors used. However, there is difficulty in implementation of analog circuits as the voltage supply is not fixed at its ends which leads to swings in small voltage.[3]

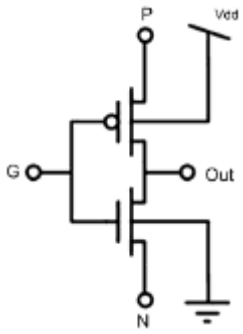

FIGURE 2: BASIC GDI CELL[7]

Different functions can be implemented by using this technique as shown in the table below. Its just a matter of understanding the concept and applying it to get the basic gates or building blocks of any digital design. For the design of vedic multiplier AND gate, XOR gate form the basis. We can design a half adder by these gates and further use half adder to make a full adder for higher designs. This technique not only saves power but also makes the design straightforward.[4]

P	N	G	Output	Function
B	'1'	A	A+B	OR
'0'	B	A	A.B	AND
B	C	A	A(bar)B+AC	MUX
'1'	'0'	A	A(bar)	NOT
'1'	B(bar)	A	(A+B)bar	NOR
B(bar)	0	A	(A.B)bar	NAND
B	B(bar)	A	A(bar)B+A.B(bar)	EXOR
B(bar)	B	A	AB+AB(bar)	EXNOR

FIGURE 3: Functions using GDI[7]

IV. PROPOSED METHODOLOGY

The design of a vedic multiplier is done by using these two techniques and then a comparison is made between them. The first one is using CMOS technology and other one is GDI technique. Both have different designs but same functionality. A comparison is done between both the techniques and different designs are presented in this paper. New techniques like quantum cellular automata(QCA) can also be merged with these techniques to increase the scope. The flow is similar, the basic gates are designed using these techniques and then they are joined to form vedic multiplier as shown.

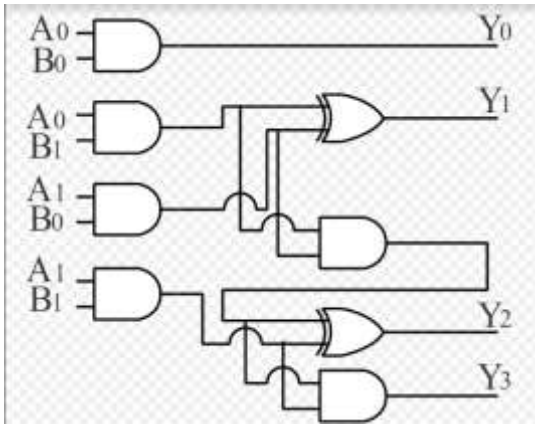

FIGURE 4: GATE LEVEL REPRESENTATION OF VEDIC MULTIPLIER

V. DESIGN OF VARIOUS COMPONENTS

AND GATE

The first step is to design an AND gate as it will perform binary multiplication. It can have multiple inputs and one output but we restrict ourselves to two inputs. In cadence we give alternating inputs which form several combinations of Vdd and 0 with the help of vpulse and we don't take same W/L

ratios of NMOS and PMOS as latter is slower than former because of its less mobility. We can also create the symbol[5]

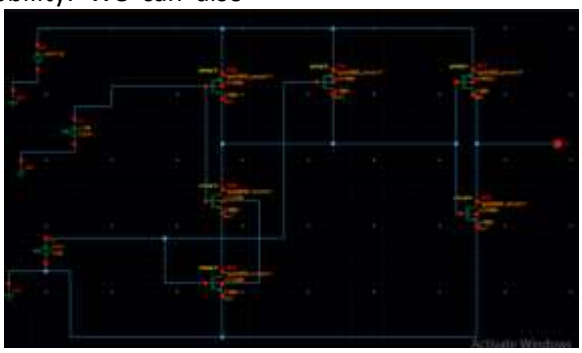

FIGURE 5: DESIGN OF AND GATE USING CMOS TECHNOLOGY

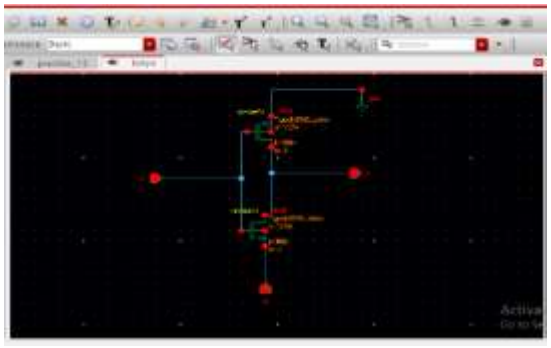

FIGURE 6: AND GATE USING GDI TECHNIQUE

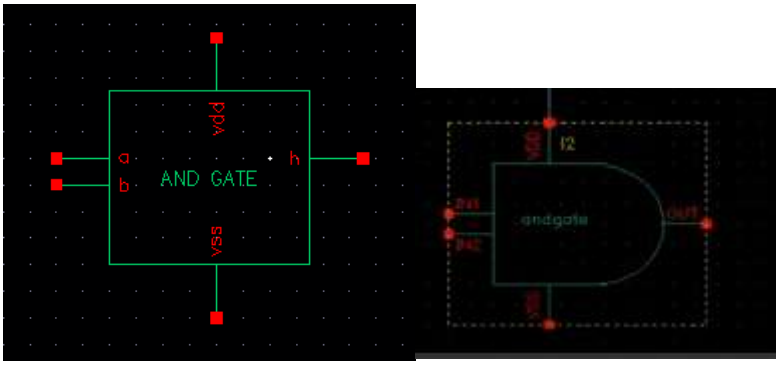

FIGURE 7: SYMBOL OF AND GATE

XOR GATE:-

Similarly the design of an XOR gate is made using both the techniques and output of this gate is high only if one of its inputs is high. Again we restrict ourselves to two input XOR gate.

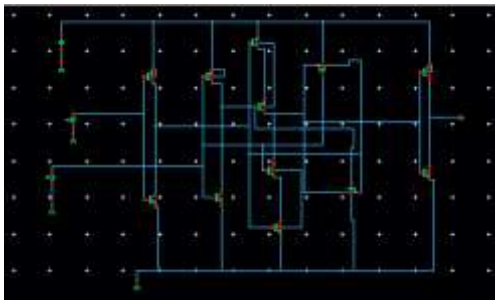

FIGURE 8: DESIGN OF XOR GATE USING CMOS TECHNOLOGY

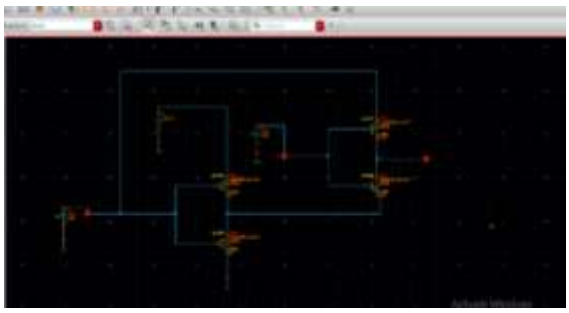

FIGURE 10: DESIGN OF XOR GATE USING GDI

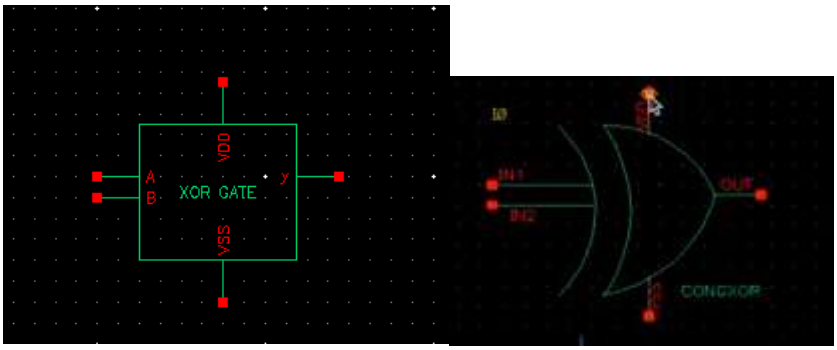

FIGURE 10: SYMBOL OF XOR GATE

NOR GATE:-

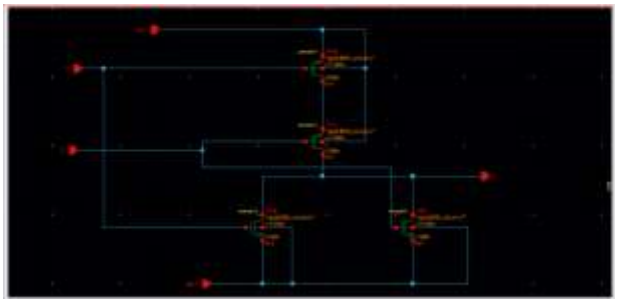

FIGURE 11: DESIGN OF NOR GATE USING CMOS TECHNOLOGY

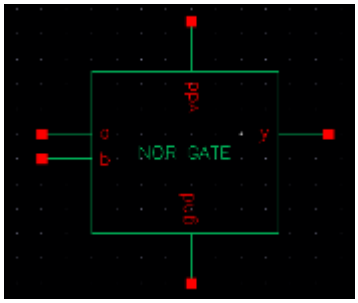

FIGURE 12: SYMBOL OF NOR GATE

HALF ADDER:-

A half adder can be made by either of the two techniques shown below.

FIGURE 14: HALF ADDER USING NOR GATES

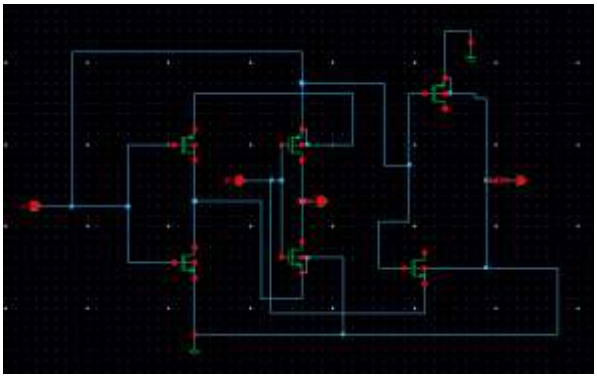

FIGURE 15: HALF ADDER USING GDI TECHNIQUE

VI. VEDIC MULTIPLIER

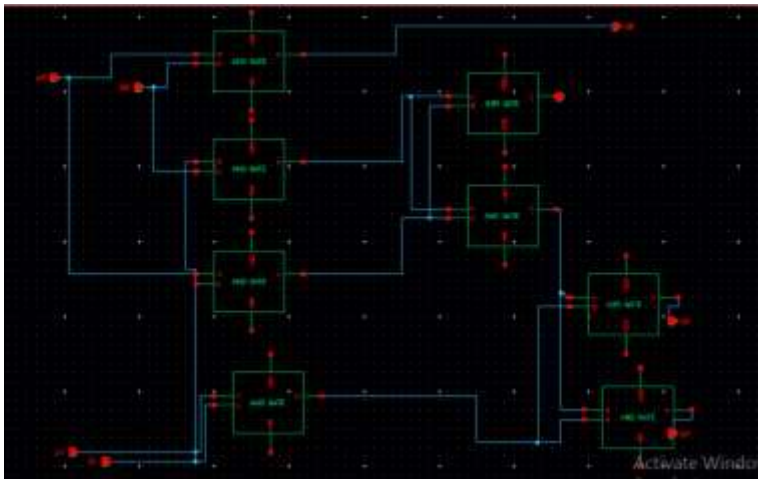

FIGURE 16: VEDIC MULTIPLIER USING CMOS TECHNOLOGY

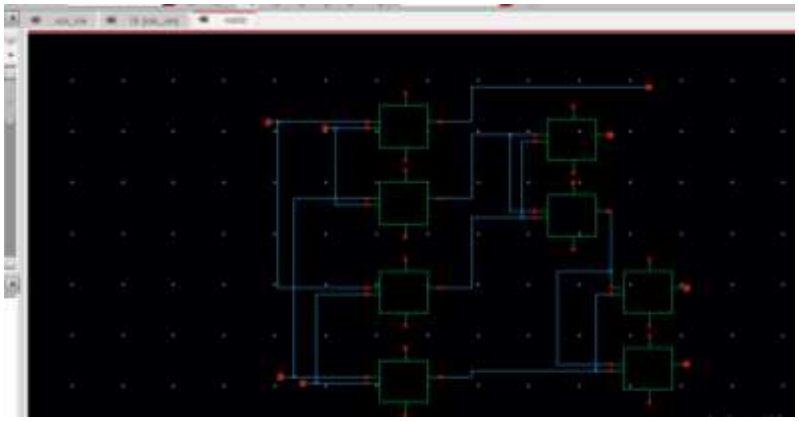

FIGURE 17: VEDIC MULTIPLIER USING GDI TECHNIQUE

VII. RESULTS AND SIMULATIONS

Various gates have been simulated and their functionalities have been verified using Cadence virtuoso. The basic design of vedic multiplier has been made using these building blocks. Vedic multiplier is a combination of AND and XOR gates, we can also use NOR and ANDgates to implement it. An important observation is made using the transient analysis which shows that the power consumed by GDI technique is less as seen inCMOS technology.

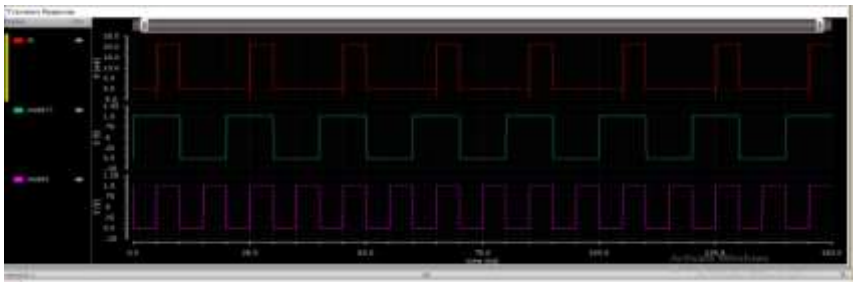

FIGURE 18: TRANSIENT RESPONSE OF AND GATE

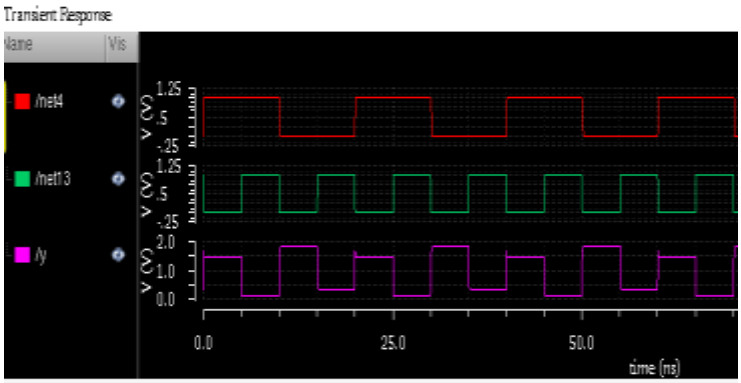

FIGURE 19: TRANSIENT RESPONSE OF NOR GATE

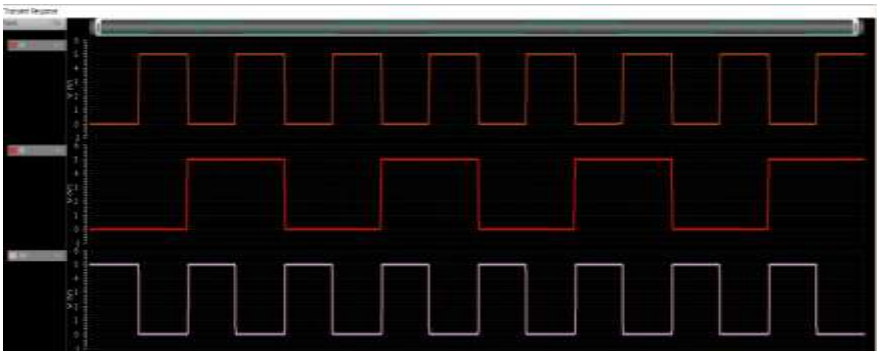

FIGURE 20: TRANSIENT RESPONSE OF XOR GATE

FIGURE 21: TRANSIENT RESPONSE OF HALF ADDER

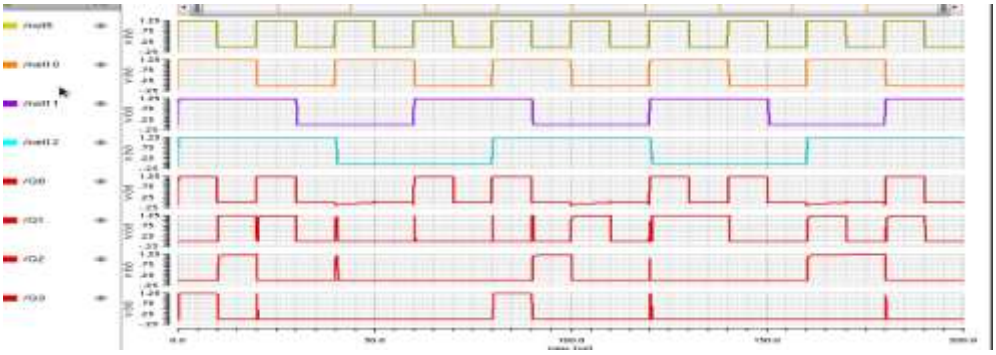

FIGURE 22: TRANSIENT RESPONSE OF VEDIC MULTIPLIER

VIII. Power dissipation (uW) comparison

SPECIFICATION	CMOS TECHNOLOGY	GDI
AND GATE	1.459	0.15
XOR GATE	1.671	0.12
HALF ADDER	5.1	0.52
2*2 VEDIC MULTIPLIER	3.66	1.66

IX. CONCLUSION

The proposed designs have been simulated in cadence virtuoso using GPDK 90nm technology. AND gate, XOR gate , NOR gate and half adder were designed using both CMOS and GDI techniques. By using these basic blocks we can make a full adder as well and extend it to high order multipliers. A 2*2 bitvedic multiplier is also made using both techniques and its power consumption is compared. It is seen that the count of transistors used in GDI technique is less as compared to CMOS technology. GDI technique also promotes low power as the power dissipation in vedic multiplier is 1.66 uW, We can also calculate the PDP in both cases. The designs of GDI technique are simpler and easy to implement. Overall performance of the multiplier has improved by using GDI

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