Low Power Clock Gated of FMO/Manchester Encoding with SOLS Method used for DSRC Applications

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***ABSTRACT*:**

In this paper, we have proposed model and it is designed using Verilog HDL and simulated using model sim software. This SOLS [Similarity Oriented Logic Simplification] improves the hardwareutilizationfrom57.14%to100%forbothFM0andManchesterencoding. In order to achieve low power consumption, clock gating is applied to the DFF. The XOR in the logic is changed tenor with the inverter, and then the NOT gate is combined with the logic forum. This shared NOT gate is moved back to the output of MUX. The delay time between both the MUX is similar to each other, so thehardwarereductionisgreatlyachievedintheproposedVLSIarchitecture.This clock gated design results in a power reduction of up to 48.7%.

Index Terms-*Dedicated short-range communication(DSRC),FM0,Manchester,VLSI.*

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I. INTRODUCTION

DSCR is aone- or two-way medium-range transmissiontechnologycreatedexclusivelyforautonomousmobilitynetworks. Two kinds of the DSRC can be distinguished with ease: automobile-to-automobile and automobile-to-roadside. For safety-related andgeneraldatabroadcasts,theDSRCpermitssignaltransmittinganddistributionamongautomobilesforautomobile-to-automobileconnectivity.Blind spot,junctionwarnings,interactsdistances,andcollision alarm are some of the safety concerns. the electronictoll collection (ETC) system, which is a form of intelligentpublic transportation[1]. With ETC, toll collection is carriedoutelectronicallyusingcontactlessIC-cardtechnology.Additionally, The ETC could be used to pay either gas andregistration expenses. As a result, the DSRC system is crucialtothecontemporaryvehicleindustry.Fig.1depictstheDSRCtransceiver's systemdesign. The upperand lower portionsareintendedforsendingandreceivinginformation,respectively. Threefundamental components make up thistransceiver:basebandcomputing,aCPU,and anRF frontend. The processor organizes baseband processing operationsby reading media access control signals also, RF front-endEncoding,transmission,faultdetection,andclocksynchronizationareallaspectsofbasebandprocessing. TheRFfront-endtransmitsandreceiveselectricaltransmissionusingtheantenna [2].

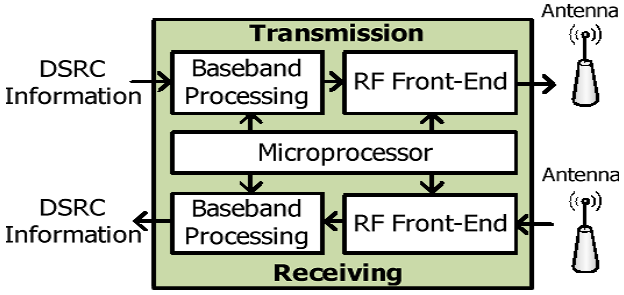

Fig.1. Design of the DSCR Transmitter Circuit.

Several groups from different countries established the DSRCspecifications. Table I lists the DSRC specifications for Tokyo,Germany,andtheUnitedStates.Theconnecti onspeedsare500kbps,4Mbps,and27Mbps,withth ecarrierfrequenciesbeing 5.8 and 5.9 GHz. Some of themodulation method utilized areorthogonalfrequencydivisionmultiplexing,qua dratureamplitudeencoding,andphase-shiftkeying.Fordurabilitypurposes, it is usual to assume that a carrier wave's amplitudehasnegligible;thisisknownasdc-balance.Unpredictablebinary sequence makes up the sent signal, this makes achievingdc equilibrium difficult [3]. The goals of FM0 andManchesteralgorithmsaretoimprovethedc-balanceofthebroadcaststream.

A. *Reviewof VLSIDesignsforFM0EncoderandMan chester Encoder*

Forvisualtelecommunications,thestudiesrecomm endaManchesterencoder VLSIdesign. TheCMOS andgatedinverterare used in this system as switches to create Manchesterencoders [4]. It utilizes 0.35-m CMOS technology and operatesat a 1GHz frequency. The architecture of one switch is furtherreplaced by the nMOS model in the literature. Their maximumworking frequency is 5 GHz, and it is implemented utilizing90-nm CMOS process. Applications involving radiofrequencyidentification(RFID),the literatureproposes ahigh-speedVLSIarchitecturethatisnearlyentirelyreusa blewithManchesterand Millerencodings.Themaximumoperatingfrequenc yforthisdesign,whichuses0.35-mCMOStechnology,is200MHz.Thisstudyalwayssu ggestsaManchesterencryptionapproachforan ultra-highfrequency(UHF)RFIDchipsimulator.

B. *SpecificationsofThisArticle*

Thecodedifferenceamongthetwo,however,substa ntially limits the ability to create a VLSI designwhich may be entirely utilized with others [5]. In thisstudy, a similarity-oriented logic simplification (SOLS)strategyisrecommendedforaVLSIstructura l layout Two fundamental techniques make up the SOLS: sharingof an area-compact range of different ways and balancinglogic operations to save 22 tr, the physical component isshiftedviaarea-compactretiming.

C. *Organization*

This essay's remaining sections are organized as the FM0andManchestercodingprinciples.

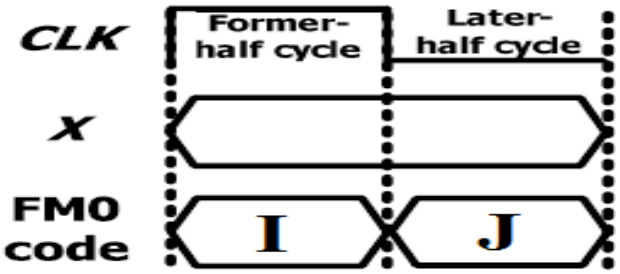

Fig. 2 FM0's design in codeword assembly of FM0.

AsshowninFig,foreachX,1theFM0codeconsistsof two parts: onefor the former half of theCLKcycle, I and theother one forthe later halfof theCLKcycle, J. Coding principle FM0 is listed as the followingthreerules.

- IfXislogical0,theFM0codemustperformswitc hingbetweenIandJ.
- If X is logical-1, no transition is allowed between themIandJ.
- A transition is assigned to each FM0 code irrespectiveofwhatX.

II. RELATED WORKS

FM0 CodeandManchesterCodeProgramming. The clock pulse and the intake info are referred to in thediscussionasCLKandX,respectively[6].Usingth eaforementioned factors, basic encoding concepts of FM0andManchestercircuitsarepresented.

A. *FM0Encoding*

Programming examination of the FM0 hardware usage.These demonstrate how challenging it is to create a VLSIarchitecture that can be used for both FM0 and Manchesterencoders. SOLS technique-based VLSI architecture design.Inthissection,KeySOLSapproachesaredesc ribed,including a region range of different ways and stabilitycircuit function sharing the analysis and findings of theexperiment.Oursectionfocusesonafaircompari sonofthisdesign to previous Manchester and FM0

encoder articles.The figure displays an example of FM0 coding [7]. The X islogic-0 at cycle 1, On its FM0 code, there is a change. Forthe purpose of simplicity, this transformation is originallyset fromlogic-0 to -1. By allocating a transition to eachFM0codeinaccordancewithrule3,logic-1isconvertedtologic-0atthestartofcycle 2.

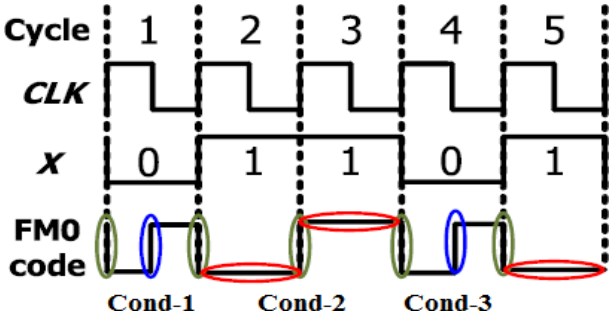

Fig.3.Figure showing an instance of FM0 programming.

Then,inaccordancewithrule2,theXoflogic-1remains at this logic level throughout cycle 2withoutanytransition. Thus,using thepreviouslygiven threeprinciples, everycycleFM0signalcanbefound.

B. ManchesterEncoding

An example of FM0 coding isshown in Fig. 2. In 1stclock period X is logic-0; therefore, it will switch to itsFM0code, according to condition 1 [8]. For simplicity,this transition is initially set from logic-0 to -1. Accordingto condition 3, eachFM0 code is assigned a transition andthus the logic 1 is changed to logical-0 at the beginning of2nd clock period. Thenaccording to condition 2 this logiclevel is held without any transition throughout 2nd clockperiodforX logic-1.TheFM0codeof each cyclecanthereforebederivedfromthesethreerules. Thetransitioncodingresultshownonthetable I&II.

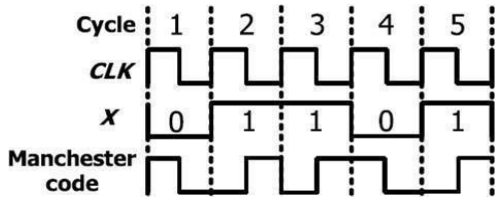

Fig 4.A representation of the Manchester programming style.

C. Limitation Analysis onHardware UtilizationofFM0Encoderand ManchesterEncoder

Similar Fig 4.A representation of the Manchester programming style. systems'physicalconfigurations theFM0 andManchester encoders are first examined before doing ananalysis on hardware use. As was already explained, theManchesterencodinghardwareimplementation isasstraightforwardasanXOR operation.Furthermore,Manchester's embedded system is simpler than FM0's [9].The FSM of 1FM0 should be used as a starting point whenconstructing the physical design for FM0 encoding.

TheFSMoftheFM0programisdividedinto4stages,asseenin Fig.5. each state receives a unique state code and eachstatecode.

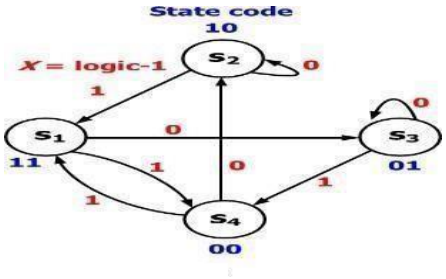

Fig.5. Representation of the FSM for FM0. (a) Designation of regions

TABLE I

Transition Table of FM0

Previous-state		Current-State			
		A(t)		B(t)	
A(t-1)	B(t-1)	X=0	X=1	X=0	X=1
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

TABLE II

HUR of FM0 and Manchester Encodings

Coding	Active Components(transistorcount)/Totalcomponents(transistorcount)	HUR
FM0	6(86) /7(98)	85.71%
Manchester	2(26) /7(98)	28.57%
Average	4(56) /7(98)	57.14%

TheBinaryfunctionalityoftheFM0programisrepresentedincludingbothA(t)&B(t).

$$\text{CLK A(t)} + \overline{CLK}\ \text{B(t)} \qquad 1$$

The Physical architectures of the Manchester and FM0encodersare displayedinFig.6togetherwith(1)and(4).Theupperportiondisplaysthe FM0encoder'selectronicsimplementation, and that of the Manchester encoder is shownin thebottom[10].Asmentioned,theManchesterencodingisas simple to use as an XOR operation for X and CLK (1).Furthermore,inaddingtotheX,theFM0encodingalsorelieson the FM0 code's prior state. The DFFA and DFFB containthe status code for the FM0 signal. The MUX-1 switches A(t)and B using the CLK channel choosing (t). A(t) and B arerealizedin(2)and(3),correspondingly(t).

Choosing the CLK indication will do this, B(t) determineswhich coding is used (2) and (3), respectively, realize A(t) andB (t) [11]. Which coding is used is determined by the modechoice made by the MUX, where Mode=0 corresponds to FM0codeandMode=1tothe Manchesterprogram.Thephysicalcomponentusagerate,whichisusedtoassesshardwareutilization, isdescribed.

$$HUR = \frac{Active\ components}{Total\ components}\ X\ 100\% \qquad 2$$

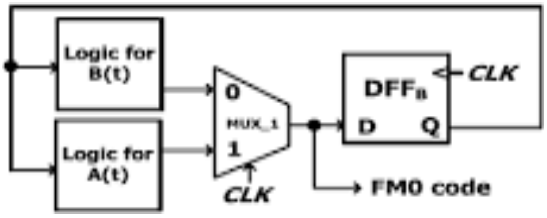

Fig.6.Region compressed retiming-free FM0 encrypting.

Thecomponent is the circuitry that performs a certainlogic operation, such asAND, OR, NOT, and flip-flop. The"active components" are thepartsthat carryout FM0orManchesterprogramming.Regardlessofthe encodingschemeemployed,thereareindeedamaximumofcomponentsintheentireembeddedsystem.

D. FM0 and Manchester encoders were designed utilizing solstechnologyinVLSIdesign.

TheSOLSmethodisbeingusedtocreatetheVLSIinfrastructure for FM0 and Manchester compression. TheseSOLS approach contains of 2 components: stability deductivereasoningcommunicationandneighborhoodpartialfulfillment.Followingisadescriptionofeachcomponentseparately[12].Finally,anassessmentoftheSOLStechnique'sperformanceisprovided.

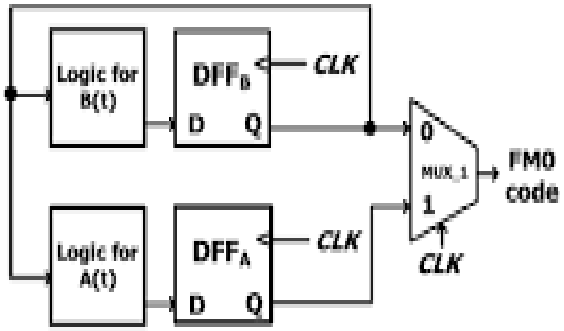

Fig.7. Postprocessing using area-compact FM0 embeddings.

Consequently,Fig.7. Postprocessing using area-compact FM0 embeddings.theB(t1)canbeencodedusingtheFM0encode utilizing only a unique 1-bit flip-flop. If somehow theDFFA is deleted properly, A(t) & B(t) these not coordinated,whichresultsintheFM0program'sreasoningandargumentation.If,asinFig6,theDFFBisthoughttobepositivelyedge-triggered,theDFFBischangedpositionfollowingtheMUX1topreventthisillogicalmistake.TheFM0 code,which consists of A and B at each phase, isderived usingthe logic of A(t) and B(t), correspondingly. Usingof MUX, this controller output of the CLK simultaneouslytoggles to FM0 code among A(t) and B(t). The Q of DFFB isimmediatelyupdated with cycle latency among the functions ofB(t) in Fig. 7. As seen in Fig, the B(t) is communicated byMUX1to theDofDFF B whenever the CLK is logic-0.Finally, this would updatefor the Q of DFFB by the impendingpositive feature of CLK. Whether the DFFB is transmitted ornot is analogous to the clockpulse for such Q of the DFFB, asrepresented in Fig 8. Consider that Table II shows the wholenumberoftransistorsandthatthe logiccomponentsof the1FM0encodingaredevelopedutilizingthelogic familyofstableCMOS. The FM0 encoding scheme

has 50 transistors overall,comparedtojust2withoutarea-compactretiming.22transistorsareeliminatedviatheregion-compactretimingmethod.

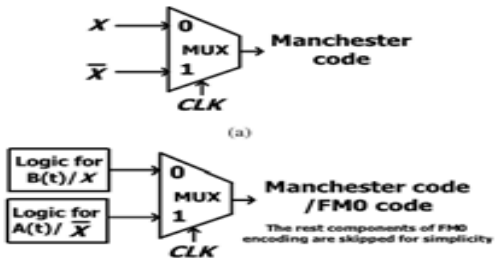

Fig.8.Balance logic operation of FM0 & Manchester.

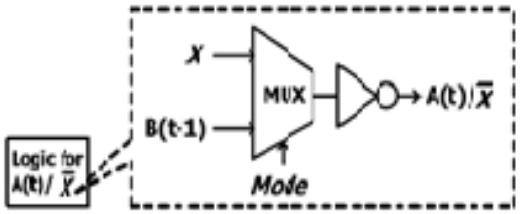

Fig.9. Logic Operation.

E. BalancingLogicandReasoningSharing

TheManchesterencryptionmaybeproducedfromX CLK,assuggested earlier, and it is similar to the X into A(t) andX intoB(t), correspondingly. Fig.10 illustrates the reasoning behindA(t)/X.

An inverter of B(t 1) can be used to deduce A(t), while aninverter of X can be used to derive X. Multiplexing is thenplaced in front of the transistor to swap the numeric values ofB(t1)andX.Thetransistorutilizedbythecircuitryf orA(t)/X canbeduplicated.WhetherFM0orManchesterencr yption is used, depending on the mode. The justificationfor B(t)/X inFigure 9 could also utilize a comparable concept(a).Manchesterencryptiondoesnotemplo ytheXOR,whichis only needed for FM0 encodes, which is a downside of thisarchitecture.Consequently,the HUR of this architecture isundoubtedly constrained. The Manchester and FM0 encodingscanbothusethe XORoperationsincethe XcouldalternativelybeeninterpretedastheX0,1.Consequently,Figure11illustrates the justification for B(t)/X, where the circuit isincharge of switching the numeric values of B(t 1) andlogic-0.Thesedesign raises theHUR by substituting theXOR foreither B(t) and X [13]. The neighborhood terminals method'srepositioned DFFB in Fig. 11 may also effectively implementmultiplexing.TheCLRisthestrongstatementthatinstructstheDFFBtorestoreitscontentsto logic-0.WhenCLRforManchesterencodingisturnedon,theDFFBcanbemade zero.The CLR is turned off when the FM0 code is used, allowingthe B(t 1) to bederived fromDFFB. As a resulting Fig. 11couldbeusedasamodulatorentirelypreserved,andtherelocated DFFB can seamlessly incorporate its function. Fig.12 depicts the suggested VLSI design for the FM0/Manchesterencoding utilizing the SOLS approach. TheMUX2 and aninverter are parts of the logic for A(t)/X. Instead, the B(t)/XlogicjustusesanXORgate.Thisprocessingefficiency of1MUX2inthefunctionalforA(t)/XandXORinthesefunctional to B(t)/X are very similar. Furthermore, this A(t)/Xcircuitryalsoincorporatesamplificationinthis MUXtwodigits.

$$= X\ \overline{CLK + CLK} + \overline{X}\ CLK \qquad 3$$

This discrepancy in computational effort among A(t)/X1andB(t)/X concludes in a bug in MUX1, which may resultin a coding error. In an effort to cut down on this imbalanceofcalculationtime,thedesignofthebalancingtimecomplexity among A(t)/X andB(t)/X.An inverter is usedto convert theXOR from the circuitry for B(t)/X to theXNOR, which is then split by the rectifier for thelogic forA(t)/X). This common rectifier is now situated at MUX 1'soutput. As a consequence, A(t)/X and B(t)/X's reasoningprocessingdurations are more uniformly distributed. Modeand CLR determine whether FM0 or Manchester codingwillbeused.TheCLRalsoperformsahardwareinitialization as a separate unique function. If the CLR isessentially generated by reversing Phase without adding aspecialCLRcontrolsignal,thereisanincompatibilitybetweenthedeviceconfigurationandtheselectionofprogramming mode. In order to prevent this conflict, it isenvisaged that both Modeand CLR will be assigned to

thisdesignindependentlyfromacontrolcircuit.

There is never any reasoning inefficiency in the suggestedVLSI architecture whether FM0 or Manchester programmingisused.BoththeManchesterandFM0 encodingsprovideeachelement's functionality. As a consequence, the recommendedVLSItechnology'sHURismuchimpr oved.

F. TimingAnalysis

Numerouslogicfamilies arecapableof realizingtheSOLS technique's logical functions. Instead of consideringdesign, every logical circuit maximizes one or more aspectsof electrical efficiencies, such as size,energy, or velocity. Inorder to achieve 100% HUR, these studied SOLS method isdesignedfromanarchitecturalstandpoint.Duetot heirgreaterintegrationindigitalcircuits,staticCMO Scircuitandtransmission-gate logic are two of the logic families that arefrequentlyused.

G. FM0 andManchesterencoders

This electronic design of the program is shown in thesebottom portions, and that of the FM0 encoder is shown inthe upper phase. The Manchester program is as easy touseas an XOR functionality to X and CLK, as stated in (1).However,theFM0encodingalsodependsonthe FM0code'sprevious state in addition to the X. The DFFA and DFFBcontain the status data for the FM0 signal [14]. The programthatisusedisdeterminedbytheMUX'smod eoption,whereMode = 0 is for FM0 and Mode= 1 is forManchesterprogram.

III. METHODOLOGY

ThearchitectureofcombinedFM0andManchestere ncodingswhichisselectedbytheMUXusingModesig nal.If Mode signal is '0' then FM0 encoding will be selected elseifMode signalis'1'thenManchesterencodingisselected.

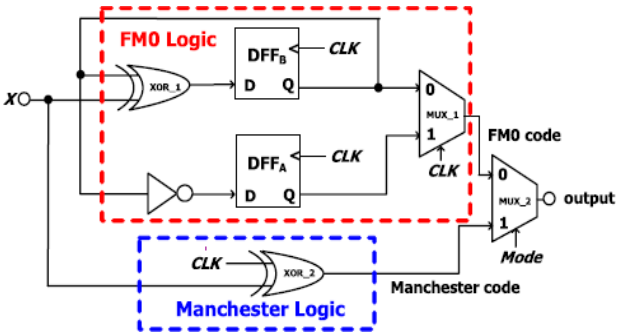

Fig.10.Hardware architecture of FM0 and Manchester encodings.

Thehardwareutilizationisthereforehigherforthec ombined design. However, the coding diversity between thesetwoisseverelylimitingthepotentialtodesign aVLSIarchitecture thatcan be fullyfunctional and mutually reused.Thispaper proposesaVLSI architecturedesign usingsimilarityoriented logicsimplification

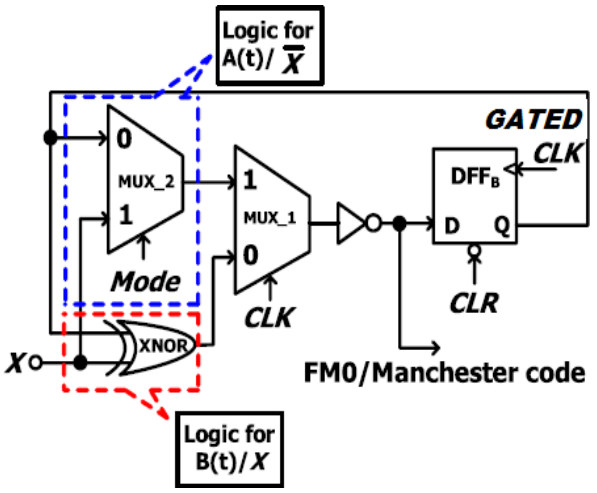

Fig. 11. Proposed Clock gated SOLS based FM0 and Manchester encodings architecture.

(SOLS)technique.SOLSconsistsoftwobasicmethod s:Area-compactovertimingandbalancinglogic-sharingoperations.Asshowninfig 10area-compactretimingrelocatesthehardwareresourcer educe22transistors.Sharinglogicandbalanceoper ationseffectivelycombinesFM0 andManchesterencodingfullyreused hardware architecture. With the SOLS technique, thispaper constructs a fully reused VLSI architecture ManchesterandFM0encodingforDSRCapplication s[15].Theexperimentalresultsshowthatthisdesig niseffectiveperformancecomparedtosophisticate dparts.

Totonedownunbalancecalculationtime,thearchit

ecture based on the computation timebetween A(t)/Xand B(t)/X is modified as shownin fig.TheXORin thelogic for B(t)/X is changed to XNOR with the inverter, andthen this NOT gate is combined with the logic for A(t)/X. Thisshared NOT gate is moved back to the outputof MUX−1. So,the delay time between A(t)/X and B(t)/X is similar to eachother. FM0 orManchester code selection relies on themodeandtheCLR.

Inaddition,theCLRcontinueshasanadditionalindiv idual hardware initialization function. If the CLR issimplyderivedbyNOToperationofthemodewith outassigninganindividualCLRcontrolsignal,thisre sultsina conflictbetween encoding mode selectionand hardwareinitialization.

To avoidthis problem, CLR and mode areassumed tobe separately assigned tothis proposal from system driver.Be it FM0 orManchester code accepted, no logical part ofthe proposedVLSI architecture is useless. Each componentis activeinbothFM0andManchesterCoding.

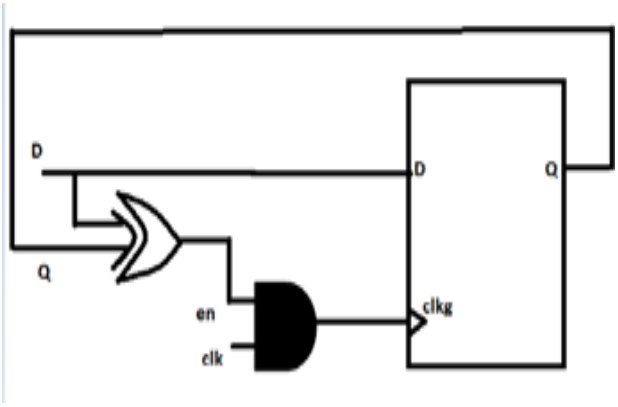

Fig.12.Architecture of DFF with clock gating logic.

Therefore, hardwarereduction isgreatly achievedintheproposed VLSI architecture. In order to achieve low powerconsumption DFF in the proposed architecture is enabledwithclockgating.Theclockconsumesmore thanhalfpercentoftheoverallchipenergy andisexpectedtoincreasein the future. This is dueto the fact thatpower it is directlyproportionaltovoltageandfrequencyassh owninthefollowingequation: $P=CV^2f$

Clockgatingworksbymakingefficient useofclocksignalbydisablingit,wheninputdataissi milartothepreviouslystoreddata. This leads to energy savings that were previously createdbyswitching states.Thisalsoresultsinasmallerdiearea,whichisn egligible.Infig.theinputandoutputoftheDFFiscom pared and when it is same the clock is disabled by ANDingthe clock with compared output. When both are same normalclockisapplied.Theclockgating architectureisshown infig.12.

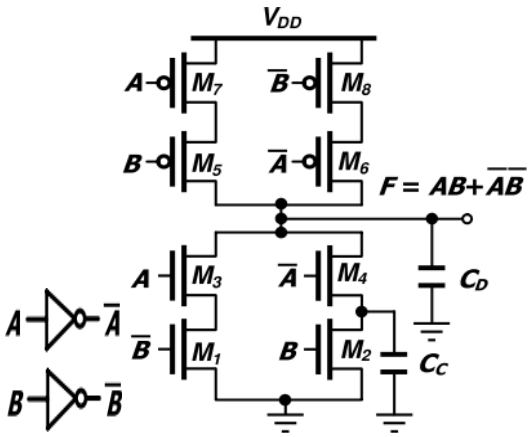

Fig.13.(a) Circuit with input variables (b) Double-input XNOR.

ForstaticCMOS,theseriesofMUX−1andMUX−2hast he upper hand in the Manchester encoded route and causes acompletelatencyas

$$2T_{MUX\text{-}SC} = 2(T_{INV} + C_A R + C_B 2R) \qquad 4$$

The circuitry designs of MUX-1, MUX-2, and XNORaccommodate for the transmitting reasoning in order tofurtherminimizethenumberoftransistorsinthe Manchesterencodingpath.Figures13(a)Atwo-inputmultiplexing and a two-input XNOR are used to illustratethetransmittingcircuitlogic,correspondingly.Thedispersiondelayofasinglebroadcasttwo-inputmultiplexingisdefinedas

$$T_{MUX\text{-}TG} = \acute{R}\, C_E 5$$

whereby the CE adds the interconnection inductance ofM1, M2, M3, and M4 combined. The R indicates to theparallelpairingofM1andM2'sorM3andM4'scor responding resistances. It is also possible to

communicatethelatencyofthetransmission-gatetwo-inputXNORas

$$T_{XNOR}\text{-}TG = T_{INV} = \acute{R}\ C_F \qquad 6$$

WherethejunctioncapacitancesofM1,M2,M3,and M4aregathered by the CF. Compared to TMUX, the TXNOR TGproduces a little bit more propagation delay. The Manchesterencoding path is dominated by the sequence of 1XNOR andMUX2inFig.13(b)fortransmission-gatefunctionality,whichresultsinatotalnetworklatencyas

$$T_{XNOR}\text{-}TG + T_{MUX}\text{-}TG = T_{INV} + RC_E + RC_F \qquad 7$$

The presumptions are listed below for a quick comparisonwith.ThetransformationofdualnMOS &dualpMOSjunctions are constantly incorporated into the CB, CD, CE,andCF1.The4capacitorswouldbeconsideredtobeCB=CD=CE=CF. Both the dual-income multiplexing & thedual-incomeXNORinstaticCMOScircuitshavetwonMOS connectedinseries.Toobtaina balancingfall-time,thewidthofthisdualnMOSinsequenceisincreasedbytwiceduration,andtheRNisisdecreasedtoRN/2.Theequivalent resistorfora transmission gate with pMOS and nMOS in parallelisRP/RN.

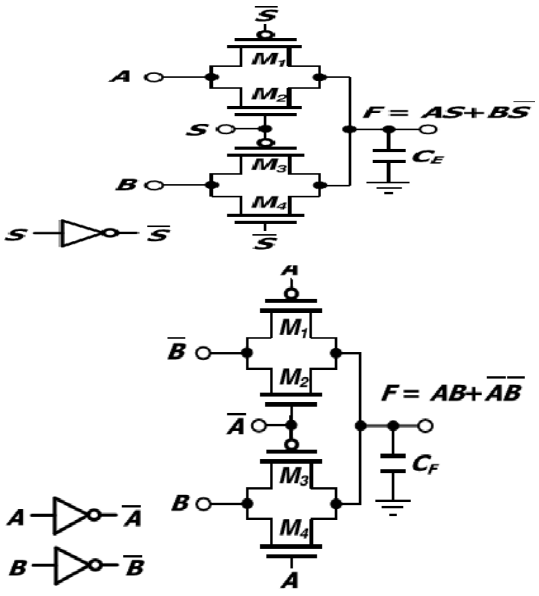

Fig.14. Circuit for transmission gates and XNOR. Circuit with two inputs (a). two-input XNOR.

A stable communication path whose RP is approximatelycomparable to RN is produced by multiplying the size of pMOSbytwotothree,accordingtothefig14.Therefore,RP/RN/RN=RN/2 is the comparable device of a transmissiongate. An nMOS in a dual-income multiplexing or dual-incomeXNORhasanequivalentresistorthatisthesameasatransmission-gate. R=R!=RN/2 is hence the assumption that isstated.

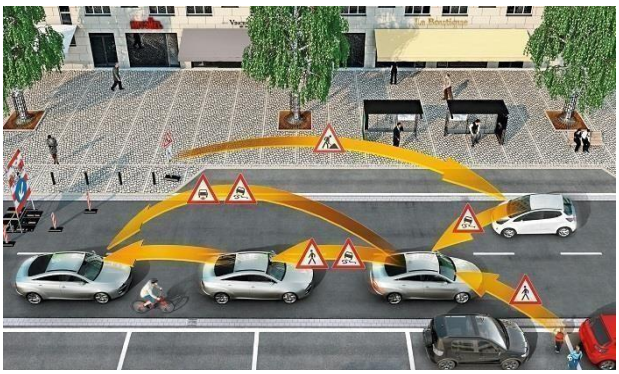

Fig.15 Short Range Communications between vehicles.

With the aforementioned presumptions, transmission-gatelogichasashorterpropagationdelaythanstatic CMOS.Infig15thetransistorcountcanbecondensed byusingtransmission-gatelogic to lessen propagation time [16]. The procedure for onereservoirimplantationfollowstherulethatperhapsthereservoiris normally placed per 3 components of transmitting circuitry.Consequently, the circuit configurations of MUX, MUX, and2MUX are developed with transmission-gate logic as a result,just two stages of transmission-gate logic areused, and thisdesigndoesnotcallfortheinsertionofanadditionalbuffer.

IV. RESULTSANDDISCUSSION

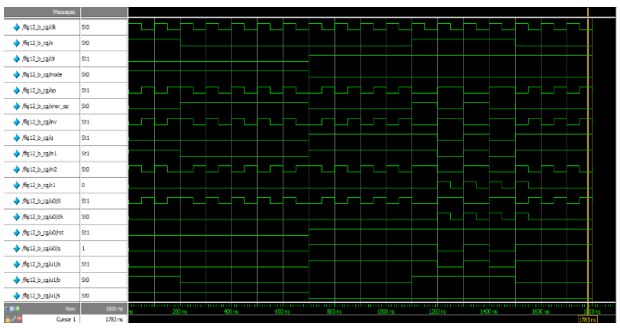

Fig. 16. Simulation result of proposed clock gated SOLS architecture for FM0 and Manchester encoding.

The simulation result of the proposed model is designed usingVerilog HDL and simulated using Modelsim software is shown infig. 16. The CLK is the input clock signal and X is the input signaltotheencoder.ModeandCLRactsasthecontrolsignal forselectingthe encoder types. OP is the encoded output. C1 is the clock gatedsignal applied to the DFF. It is '0' and does not make any transitionforthesimilardata.

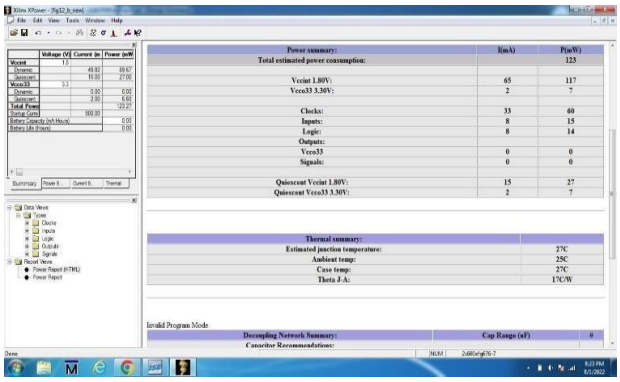

Fig.17. Power report of existing SOLS architecture for FM0 and Manchester encoding without clock gating.

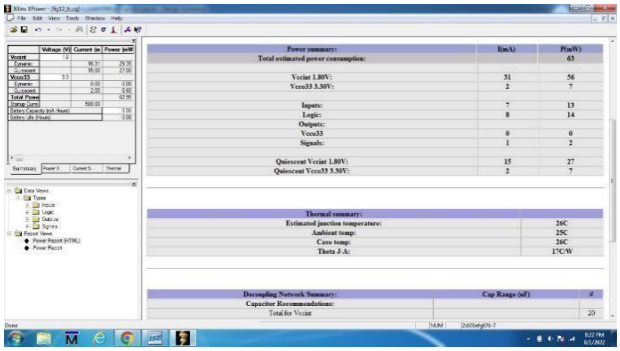

Fig.18. Power report of proposed clock gated SOLS architecture for FM0 and Manchester encoding.

Fig.17 and Fig 18 shows the power result of existingandtheproposeddesigns.TheVerilogcodeissynthesizedin XilinxFPGAfor analyzing thepowerresults. Compared to the existing design the proposedworkresultsinalmost49%ofpowerreduction.

V. CONCLUSION

The equipment use of the VLSI engineering plan ishamperedby thecoding-variable characteristics of theFM0 and Manchester programming's. This work proposesaproductivereusableVLSIengineeringapproachutilizingSOLStoeitherFM0andManchesterprograming.SOLStechnologyimproveshardwareutilizationfrom57.14%to100%forbothFM0andManchester encoding. These SOLS technology removesupequipmentusagerestrictionusingtwocentraltechniques:adjustrationaloperationsharing andterritorial minimal retiming. The industrial asset is movedto use 22 fewer transistors due to the range-minimizedrange of different ways. With the help of easily distinctreasoningcomponents,theadjustrationale operationsharing successfully consolidatesFM0 andManchesterprograming. The highest possible operating intensity forManchesterandFM0powerreductionupto48.7 %.

VI. REFERENCE

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