Modify Two Stage OPAMP based on Offset Constellation Technique

Firas Sami Abdul-Kadhim[1], Hassan JassimMotlak[2]
[1,2]Department of Electrical Engineering, Babylon University, Iraq
firas22sami@gmail.com

ABSTRACT

The main objective behind this proposed design is to reduce the low offset voltage for the minimum value, so that its effect is reduced by two stage CMOS operational amplifier. The majority of operational amplifiers mainly consist of two inputs and one output. The signal coming out from the amplifiers is a description of the distinction and comparison between any two input signals that are independent on each other. Practically no voltage appears on the output and the offset voltage is close to zero in the event that there is no difference between the two input signals. In this paper, comprising two proposed circuits are designed and simulated using OrCAD PSpice 17.4, first, a circuit consisting of two stages is designed for a 180 nm technology operational amplifier, a designed two-stage amplifier circuit consisting of eight semiconductor switches (MOSFET). Second, a proposed circuit consist of a two stage OPAMP in conjunction with an auxiliary OPAMP, In the two proposed circuits, the MOSFET parameters are designed and excellent results obtained, including reduction of offset voltage and preservation of the gain value, where the offset voltage value of the Two-stage circuit was 71µv and the offset value of the proposed design was equal to 21µv as the offset voltage was improved and reduced by 70 %.

Keywords:Offset voltage,OPAMP, CMOS, Auxiliary OPAMP,Constellation Technique.

DOI Number: 10.14704/nq.2022.20.3.NQ22342 NeuroQuantology 2022; 20(3):520-539

1. INTRODUCTION

Nowadays, all electronic devices have become directly and fundamentally dependent on OPAMPs, as most scientific and consumer applied devices use wide ranges of these amplifiers and with most applications Nowadays, all electronic devices have become directly and fundamentally dependent on OPAMPs, as most scientific and consumer applied devices use wide ranges of these amplifiers and with most applications [1], An op amp employing two or more gain stages is widely used when higher gains are required[2],MOSFET Of the electronic elements widely used in analog circuits, one of the most important advantages MOSFET is small in size, more than 10 times faster than transistors, and the effect of heat in it is less and the opening current is smaller compared to the transistor[3] When a mismatch occurs between the components of the CMOS, a so-called offset voltage appears, and this affects the resolution and speed of the device[4], and there are two types of offset voltages, namely input offset

voltage(IOV)and output offset voltage(OOV), the first is preferred in applications with high resolution and the second in applications that have a high speed[5]. There are several ways to eliminate the offset voltage, auto-zeroing method, chopping ,trimming and correlated of the double sampling etc.[6], noise folding the disadvantages of auto-zeroing, ripple the disadvantages of chopping. As for the proposed design, we were able to overcome these problems. The aim of this paper is to reduce the offset voltage, which mainly affects speed and resolution, while maintaining circuit stability Designs were made using the Orcad P-SPICE program (17.4)2019 and using the 180 nm technology. Two designs were made, the first is the design of the two-stage op-amp circuit, the simulation of the circuit was made and the results were extracted, and the results showed an improvement in the offset voltage value, as for the second design, it is modify two stage ,the same as the first design with the addition of an auxiliary amplifier that connects to the feedback of the circuit. The benefit of it is to reduce the offset value, and actually, through simulation, the offset voltage value was improved by 70 % over the first design.

Daniel DZAHINI and Hamid Ghazlane (2002), in this paper, the design was designed using 800 nm technology, with an input voltage from 2 uV to 100 nV and the source voltage is 2.5 V and the value of the bandwidth was 2 MHZ, and the method used is continuous time of auto-zero [7]

Masaya Miyahara and Akira Matsuzawa (2009), the design was done using a new dynamic, and the proposed design achieves a low offset voltage. The 90 µm technology was used and it achieved good results in the design, as the value of the offset voltage was 3.8 volts with a voltage source of 1.2 at 500 MHz [8]

Heung Jun Jeon and Yong-Bin Kim (2010), the proposed design of the comparator that is used to reduce the offset voltage, and two inverters were added and were placed between the input and the output stage, the design was achieved by 90 nm with a 1V voltage source, the displacement voltage improved by 19 percent and less sensitivity by 62 percent.[9]

Heung Jun Jeon et al (2011), The dynamic comparator was analyzed and according to this analysis, the offset voltage value was reduced from I2.5mV to 6.5mV with an increase in the energy dissipated value of 9%. Witt using capacitive offset calibration, using a digitally the controlled the capacitive offset for the calibration technique through technology, the offset was reduced to I.10 mV after it was6.5mV [10]

Chi-Hang Chan et al (2011) Low-noise designs were presented and the offset value was low, and the comparator ADC was used to reduce noise and offset, as the offset was improved from 11.6mV to 533µV and was done using 90 nm technology at a frequency 1.5GHzand the power supply 1.2V[11].

Heung Jun Jeon and Yong-Bin Kim (2012), the comparator of the dynamic latched with the offset voltage, the comparator need one clock signal for operation and the result the gain is 22, power supply 1V and using 90 nm technology offset voltage is reduced 24.6% less from (6.03 -1.1) mv [12].

Samaneh Babayan-Mashhadi and Reza Lotfi (2012), A new method was used to cancel the offset, and this method is to adjust the body's voltage by using a circuit analog with control feedback with low-power, the 0.18 nm technology is used with 1.8V power supply the offset is decreasing (36.2 to 7.1) mV [13].

Mohsen Hassan pourghadi et al (2013), in this paper, the comparator was designed with positive feedback, the mismatch that occurs between the circuits determines the ratio between speed, offset and energy consumption, the design was done using 180 nm and 90 nm technology, and the resulting offset value was one-third of the value and the energy consumption value was 44 percent

power consumption is 51uW and the offset voltage is 15.1mV [14].

MeysamMohammadiKhanghah and KhosrovDabbaghSadeghipour, (2014) A new high-speed design comparator has been proposed, using A new boost method, simulated by Montecarlo method, using 180 nm technology, power dissipates 34 uW, voltage source is 0.5 and the offset voltage value is 0.288mV [15].

V. Raghuveer et al (2017), In this paper, a mechanism for reducing offset voltage is discussed, using a continuous of the zero-automatic amplifier, and an offset voltage of 2microvolt was obtained and the gain value was 131 dB, the bandwidth was 1.5 MHZ and the power supply was 1.8 volt [16].

L.Kouhalvandi (2017), in this paper, the comparator was designed that enjoys high speed and accuracy, and the design was made using 180 nm technology and a voltage source of 1.8 volts, the monticarlo method and angle and the use of 100 samples and 9 angles were used, and this design is suitable for use in conversion from analog to digital in electronic applications [17].

Avaneesh K. Dubey, and R.K. Nagaria (2018), designed CMOS with low power high-speed the used bulkdriven method., this method for low power result in reduced transconductance, the used 45 nm CMOS technology and with 0.8V power supply the offset voltage is 1.05mv [18].

P.P. Gandhi and N. M. Devashrayee (2018), The comparator was designed to obtain a better improvement in the value of the offset voltage, and the results were verified by Monte Carlo, and the results showed that the proposed system is 45% faster and the rate of improvement of the offset voltage is 91%, and it was done using 180 nm technology and a voltage source of ± 0.9 [19].

G¨unhanD¨undar et al (2019), designed the circuit for determine direct current (DC) offset cancellation (OC) on the amplifier subject to aging and an identifier of his performance percentage the designed in low power with 40 nm Technology and power supply is 1.1 V the gain 22.2 dB and offset voltage 14.42mv [20].

Robert Chen-Hao Chang et al (2019), designed a low offset voltage by used a constant on–time buck converter with 3.3V power supply and using 0.18um CMOS technology, the reduced the offset voltage to 8mv with high efficiency93.4 % [21].

KasiBandl et al (2020) The are design circuits using successive approximation register (SAR) – ADC (analog to digital converter) the was used 180 nm CMOS technology with power supply 1.8V and the offset voltage is 6 mv [22].

EmadAlnasser (2020) was proposed circuit for reduce the Offset Voltage of the output he used conventional charge of the amplifier to reduce the offset the gain of the circuit is 20.5 dB and the offset voltage of output 5mv [23]

1. Modeling and characteristics of operation amplifier (OP-AMP)

Operation amplifier is one of the most used electronic parts in most fields and in the IC industry and in most electronic devices for several reasons that are important at the same time, including its small size, does not require high currents and does not consume high power [24] , and you can find the operation amplifier in one or two phases, depending on the use you need, and it is also used as a comparator, or for other parameters such as addition or subtraction and many more [25].

2. Conventional CMOS two stages operation amplifier

The circuit shown in fiq (1) was designed with a 180 nm technology and the circuit was designed by Orcad 17.4 software, and in order to design a circuit of tow stage you must follow the following methods. selecting

eISSN 1303-5150

the basic structure of the op amp, choosing of the dc currents and MOSFET sizes and Choose the parameters and know their measurements.

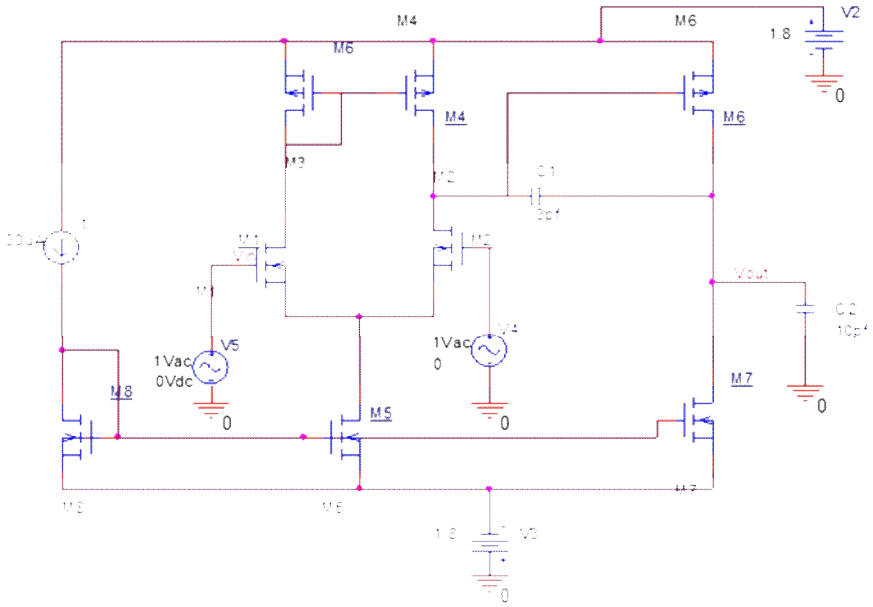

Figure1. Schematic the Tow stage Operation Op Amp circuit.[26]

3.1. First, the principal equation has to be extracted by Kirchhoff Current law (KCL)[27,28]

$\frac{v_o}{v_i} = \frac{A_{DC}(1-\frac{s}{z})}{1+s(\frac{1}{p_1}+\frac{1}{p_2})+s^2(\frac{1}{p_1 p_2})}$(1)

Input pole, $P_1=\frac{1}{g_{m2}r_{o2}r_{o1}c_c}$(2)

Output pole, $p_2=\frac{g_{m2}}{c_2}$(3)

Zero Z=$\frac{g_{m2}}{C_c}$ (4)

Slew rate SR = $\frac{I_5}{C_c}$ (5)

Voltage gain $A_{DC}=g_{m1}g_{m2}r_{o1}r_{o2}$ (6)

Gain Band width, GBW = $\frac{g_{m1}}{c_c}$ (7)

Some specifications are fixed and must be placed before the design in the tow-Stage circuit, such as slew rate, gain Bandwidth, and others as shown in Table 1.

Table 1. Fixed specification with circuit design of the CMOS two stages op amp

parameter	value
Power supply	±1.8
Slew rate	10 V/μs
Channel length	180 NM

Load capacitance 12 pF	10 pF
$\mu_n c_{ox}$	110 μA/V²
$\mu_p c_{ox}$	50 μA/V²
Gain Bandwidth	5 MHZ
Phase margin	60°

1.2. The Design Calculate the ratio between width to length of the all CMOS MOSFET in the circuit[1,3]

$C_c = \frac{2.2}{10} C_L$ (8)

$I_5 = SR(C_C)$, $g_{m1} = GB(C_c)$ (9)

$S_{1,2} = (\frac{W}{L}) _{1,2} = \frac{g^2 m_1}{(K^-1)(I_5)}$ (10)

$S_{3,4} = (\frac{W}{L})_{3,4} = \frac{I_5}{(K^-_3)[V_{DD} - V_{in}(max) - |V_{To3}|(max) + V_{T1}(min)]^2}$ (11)

$V_{Dss} = V_{in}(\min) - V_{ss} - \sqrt{\frac{I_5}{\beta_1}}$ - $V_{T1}(\max)$ (12)

$S5 = (W/L)5 = \frac{2(I_5)}{K^-_5 \ (V_{Dss})^2}$ (13)

$g_{m6} = 2.2(g_{m2})(C_L/C_c$ (14)

$S_6 = (\frac{W}{L})6 = S_4 \frac{g_{m6}}{g_{m4}}$ (15)

$I_6 = \frac{g^2_{m6}}{2 K^-_6 S_6}$ (16)

$S_7 = (\frac{W}{L})7 = S_5 \frac{I_6}{I_5}$ (17)

The final values and results obtained through the design process are indicated in the final Table 2.

eISSN 1303-5150

MOSTET	W/L ratio	Width(W)(μm)	Length(L)(μm)
M1, M2	3	0.54	0.18
M3, M4	15	2.7	0.18
M5, M8	4	0.8	0.18
M6	94	17	0.18
M7	14	2.5	0.18

Table 2. MOSFET ratio and width of all transistor

The Table shows the values of the ratio of (W/L) obtained according to the above equation, these values were calculated manually and according to the equations

4 The proposed circuit

In this part of the research, it is in two parts The first part is the Architecture of the proposed circuit, second part is Schematic of the proposed circuit

4.1 Architecture of the proposed circuit

The figure (2) shows the proposed design that consists of several parts to form the final design, which consists of (Gmi) , which is a differential pair, also consists of a resistance (R1) which is the load and consists of (A2) which is a second amplifier, all these three elements that we mentioned represent Know the two stage , It also consists of the auxiliary amplifier(Aaux) and the (Gm, aux) which act as a feedback to the circuit , Vos1 represents the voltage applied to the main amplifier circuit and the second voltage VOS2 is the primary voltage of the auxiliary circuit, and these two voltages are the input to the circuit , the role of the switches is open during an operation canceling , In the following equations that link the input and output voltages

$$\pm V_{os1}G_{m1} - (V_{in}^{+} \pm V_{os2}V_{out})A_{aux}G_{m,aux}]R_1A_2 = V_{out} \quad (18)$$

$$V_{out} - V_{in}^{+} = V_{os2} \pm \frac{V_{os1}G_{m1}}{A_{aux}G_{m,aux}} \quad (19)$$

The capacitor (C) performs the process of storing the voltages of (A aux) and the switches in this state are closed and the voltage value is as follows.

$$V_{out,tot} = \frac{V_{out} - Vin_{in}^{+}}{G_{m1}R_1} \quad (20)$$

$$V_{out,tot} = \pm\frac{V_{os2}}{G_{m1}R_1} \pm \frac{V_{os1}}{G_{m1}R_1A_{aux}}\left[\frac{G_{m1}}{G_{m,aux}}\right] \quad (21)$$

If the A(aux)

$$A_{aux} = \frac{G_{m1}}{G_{m,aux}} \quad (22)$$

Then the output offset voltage equal to the equation

$$V_{os,tot} = \frac{V_{os1}}{G_{m1}R_1} + \frac{V_{os2}}{G_{m1}R_1} \quad (23)$$

$$V_{out,tot} = \frac{1}{G_{m1}R_1}(\pm V_{os2} \pm V_{os1}) \quad (24)$$

So that we get the lowest error, the values of (Gm, aux) are much less than the value of (G mi) and the voltages are very small until a match occurs with the devices, depending on the two equations

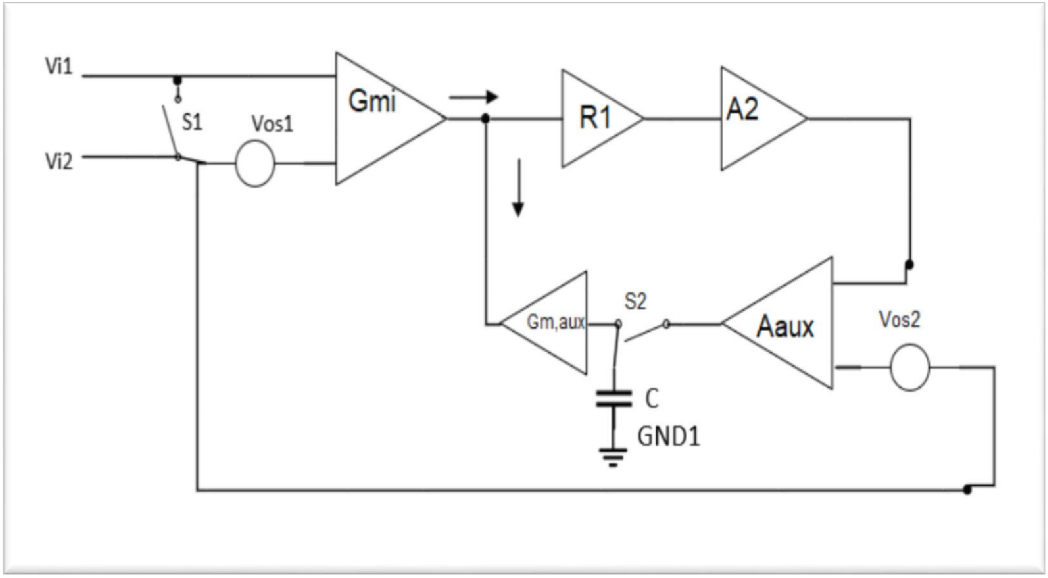

Figure 2. Architecture of the proposed circuit cancellation technique

Table 3. The ratio of (W/L) proposed of two stages CMOS with cancellation technique

MOSTET	W/L ratio	Width(W)(μm)	Length(L)(μm)
M1, M2	3	0.54	0.18
M3, M4	15	2.7	0.18
M5, M8	4	0.8	0.18
M6	94	17	0.18
M7	14	2.5	0.18
M9	3	0.54	0.18
M10, M11	94	17	0.18
M12, M13	14	2.5	0.18
M14	4	0.72	0.18

The Table shows the values of the ratio of (W/L) of the proposed circuit with cancellation technique

4.2 Schematic of the proposed circuit

In the design shown in figure (3), the proposal consists of (M5, M2, M1) where this part represents (G mi), M3and M4 where it represents these two transistors (R1) and the transistors M6 and M7 represent the (A2), as well as representing a group Transistors (M9, M10, M11, M12, M13) the auxiliary amplifier and finally the transistor (M14) represents the (Gm, aux

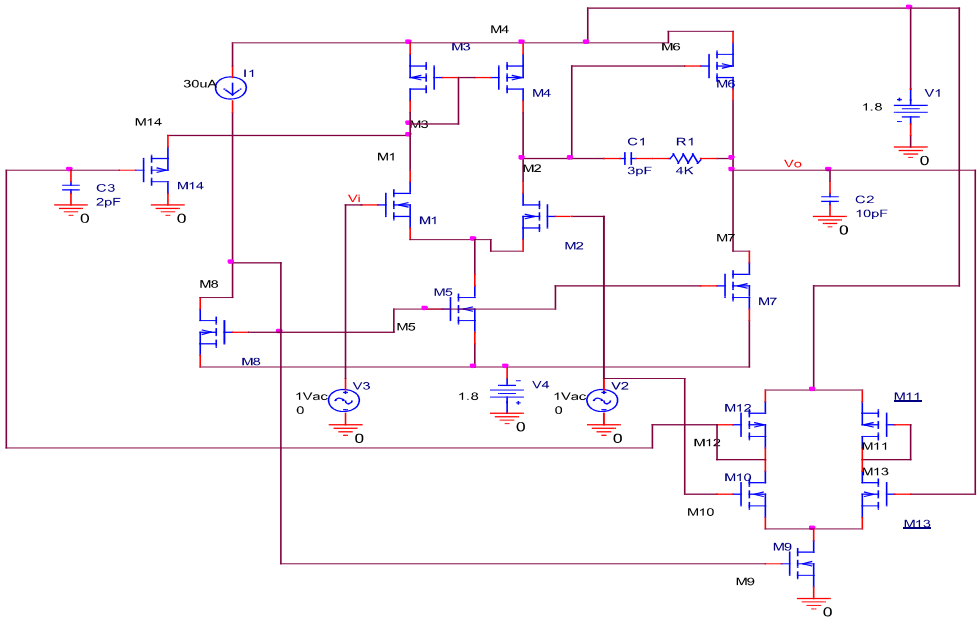

Figure. 3 Schematic of the proposed circuit with cancellation technique

5. Results of the proposed two stage cancellation technique

In this part of the research, the same previous equations will be used in the two -stage circuit, the design was made with a technique of 180 nm and a voltage source of 1.8 volts the designed by P-Spice 17.4 software, In the following tables, the first Table 4 shows the results for the first design of the Two-stage op-amp, the second Table 5 shows the results for the second proposed design of Two-stage with cancellation technique.

Table 4. Performance Parameters of The Two Stage CMOS Op-Amp

Performance Parameters	Value with unit
DC Voltage Gain	77 dB
Gain Bandwidth	4.7MHz
Bias Current	30 µA
settling time	170ns
Slew rate	42 v/µs
Offset Voltage	71µV

Supply Voltage	±1.8V
Phase Margin	65◦
DC Power Dissipation	0.446 mW

The table shows most of the parameters that were extracted by the p spice program, such as gain, offset voltage, slew rate and others,notice that the phase margin value is greater than 45, which means that the system is stable

Table 5. The result of the proposed of two stages CMOS with cancellation technique

parameter	The amount
Power supply	±1.8V
DC Voltage Gain	77dB
phase	180 degree
Gain bandwidth	4.9 MHZ
settling time	116ns
Slew rate	42 v/µs
Phase margin	87
Offset Voltage	21uV
Power dissipated	0.4mw

The table shows most of the parameters that were extracted by the p spice program, such as gain, offset voltage, slew rate, offset Voltage and others with cancellation technique.

The AC analysis gain and gain bandwidth shown in fig. 4, phase, phase margin, settling time, slaw rate in the following two figures. 5, 6 and the offset voltage is reducing to be its value equal to 21µv after it was equal to 71µv, the values of capacitance and resistance are equal to 4 Kohm ,3pF respectively, and as placed in the shapes before and after the process of cancellation technique.

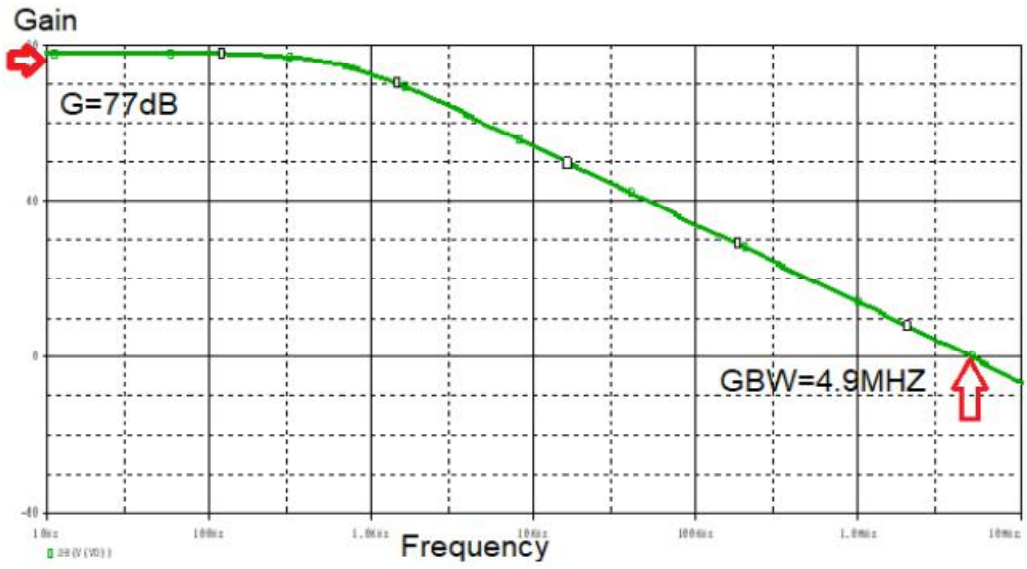

Figure 4. Simulation Result of frequency response for Two-stage CMOS Op-Amp with cancellation technique (Gain and gain bandwidth)

The Simulation Results, we notice that the gain value is equal to 77dB and unity gain band width is 4.9MHZ

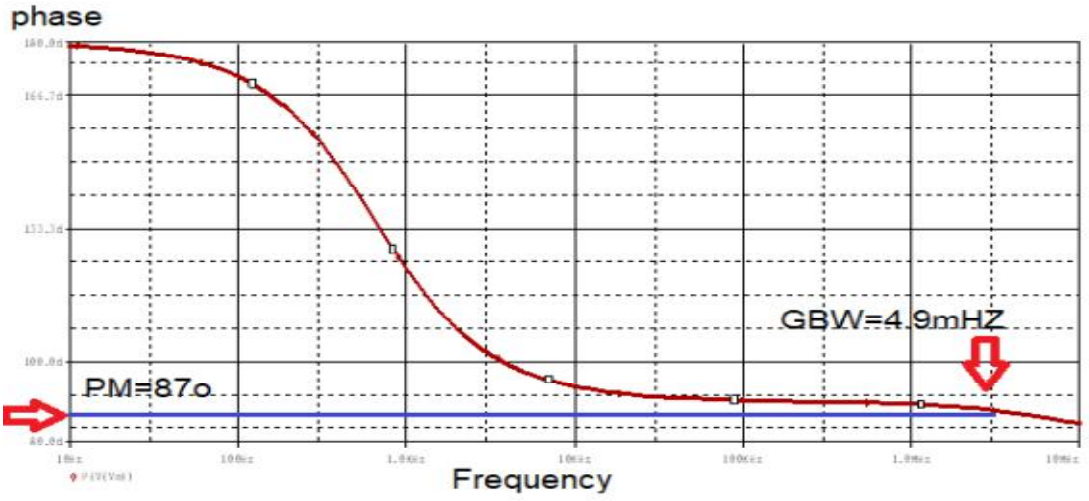

Figure 5. Simulation Result of frequency response for Two-stage CMOS Op-Amp with cancellation technique (phase and phase margin)

The Simulation, we notice that the phase equal to 180 degree and the phase margin is 87 degree, and note that the phase margin is grater thar 45 degree that's main the system is stable.

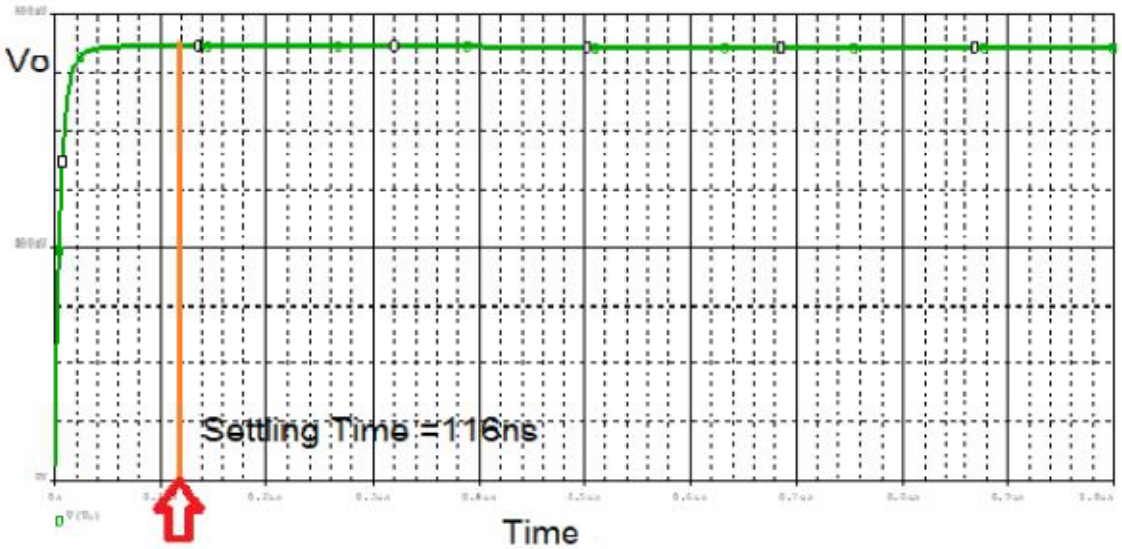

Figure 6. Simulation Result of Two-stage CMOS Op-Amp with cancellation technique (slaw rate and settling time)

The simulation Result, notices that the slaw rate of the Two -stage is 42 v/µs , settling time value is 116ns.

We conducted a comparison between the proposed design and previous studies with the same technique, as it can be seen that there is a significant improvement in the value of the displacement voltage as shown in the Table 6,

Table 6. Comparison between the proposed work and related previous works

parameter	Proposed work	[15-2018]	20-2019]	[22-2020]
Technology	180NM	180NM	40nm	180NM
Power supply	±1.8V	±1.8V	1.1v	1.8V
gain	76dB	11.5dB	21.26 dB	-
Offset Voltage	21 µV	52.58mv	14.41mv	6mv
Power dissipated	0.4mw	-	6-2019	4.72µW
Phase margin	87	89	45◦	-

530

Through the table, the results showed that there was a significant improvement in the amount of the offset value, and by comparison with it, previous work showed that the department proposed by us was the value of the improvement in it.

6. CONCLUSION

The offset voltage cancellation process, which we mentioned earlier, occurs due to the mismatch of the parameters of the circuit. It is applied to the two-stage op-amp circuit it was done using 180 nm technology, and the value of the offset voltage was equal to 21 µV the larger the capacity of the capacity, the smaller the offset voltage value, Whenever the Rds value of transistors (M6)and (M7)increases, the offset voltage value decreases

REFERENCES

[1] S. Bandyopadhyay, et al, “Design of Two Stage CMOS Operational Amplifier in 180nm Technology with Low Power and High CMRR”, *International Journal on Recent Trends in Engineering & Technology*, Vol. 11, PP 239-247, 2014

[2] R. B. Reddy and Sh. K. Gowda, “Design and Analysis of CMOS Two Stage OP-AMP in 180nm and 45nm Technology”, *International Journal of Engineering Research & Technology (IJERT)*, Vol. 4, PP 1100-1103, 2015

[3] R. Chaudhari and R. Soni, "Design and Characterization of two stage High-Speed CMOS Operational Amplifier", *Rahul Chaudhari et al Int. Journal of Engineering Research and Applications*, Vol. 4, PP. 536-541, 2014.

[4] M. J.M. Pelgrom, et al,"Transistor Matching in Analog CMOS Applications, ", *in Applied. of Technical Digest of International Electron Devices Meeting, Cat. No. 98CH36217*, pp. 915-918, 1998.

[5] S. Alam Chowdhury, et al, “Design of a Two Stage CMOS Operational Amplifier in 100nm Technology with Low Offset

Voltage", *In: Applied. Of International Conf. On Innovations in Science, Engineering and Technology (ICISET), Chittagong, Bangladesh*, PP.56-59, 2018

[6] J-Y. Zhang, et al, "Design of low-offset low-power CMOS amplifier for biosensor application ",*Journal of Biomedical Science and Engineering*, Vol.2, No.7, pp. 538-542, 2009.

[7] D.DZAHINI and H. Ghazlane," A very low offset voltage auto−zero stabilized CMOS operational amplifier", *Workshop on Electronics for LHC Experiments 8*, pp. 1-3, (2002).

[8] M. Miyahara and A. Matsuzawa, "A Low-Offset Latched Comparator Using Zero-Static Power Dynamic Offset Cancellation Technique", *in Applied of sian Solid-State Circuits Conference*, pp. 233-236, (2009).

[9] H. Jeon and Y.gBin Kim, "A CMOS LOW-POWER LOW-OFFSET AND HIGH-SPEED FULLY DYNAMIC LATCHED COMPARATOR", *in Applied of International SOC Conference* , pp. 285-288, (2010).

[10] H. Jeon ,et al, "offset Voltage Analysis of Dynamic Latched Comparator", *In International Midwest Symposium on Circuits and Systems (MWSCAS)* ,pp. 1-4, (2011).

[11] Ch. Chan, et al, "A Reconfigurable Low-Noise Dynamic Comparator with Offset Calibration in 90nm CMOS", *in Applied of Asian Solid-State Circuits Conference*, pp. 233-236, (2011).

[12] H. Jun Jeon and Y. Kim, "A novel low-power, low-offset, and high-speed CMOS dynamic latched comparator", *Integrated Circuits and Signal Processing*, Vol.70, No. 3, pp.337-346, (2012).

[13] S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming" *Analog Integrated Circuits and Signal Processing*, Vol. 73, No.3, pp. 673-682, (2012).

[14] M. Hassan pourghadi, et al, "A low-power low-offset dynamic comparator for analog to digital converters", *Microelectronics Journal*, Vol. 45, No.2, pp. 256-262, (2014).

[15] M. MohammadiKhanghah and K. DabbaghSadeghipour, "A 0.5 V offset cancelled latch comparator in standard 0.18 lm CMOS process", *Analog Integrated Circuits and Signal Processing*, Vol. 79, No.1, pp. 161-169, (2014).

[16] V. Raghuveer, et al, "A 2µV Low Offset, 130 dB High Gain Continuous Auto Zero Operational Amplifier", *inAppliedofS International Conference on Communication and Signal Processing*, pp. 1715-1718, (2017).

[17] L. Kouhalvandi, et al, "10-bit High Speed CMOS Comparator with Offset Cancellation Technique", *Workshop on Advances in Information, Electronic and Electrical Engineering (AIEEE),* pp. 1-4, (2017).

[18] A. K. Dubey and R.K. Nagaria, "Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A low-power, high-speed design approach using bulk-driven load", *Microelectronics Journal*, Vo.78, pp.1-10, (2018).

[19] P.P. Gandhi and N. M. Devashrayee, "A novel low offset low power CMOS dynamic comparator", *Analog Integrated Circuits and Signal Processing*, Vol. 96, No.1, pp. 147-158, (2018).

[20] D. Erol, A. Do˘gus¸ G¨ung¨ord¨u, G. D¨undar and M. BerkeYelten "An Offset Cancellation Set-up for Amplifiers Subject to Aging", In: Proc. Of International Conference on Electrical and Electronics Engineering (ELECO) ,pp. 384-387.(2019).

[21] R. Chen-Hao Chang, et al, "A 93.4% Efficiency 8mV Offset Voltage Constant On -Time Buck Converter with An Offset Cancellation Technique", *Transactions on Circuits and Systems II*, VOL. 67, No. 10, pp.2069- 2073, (2019).

[22] K. Bandla, H. krishnan, and D. PalSMIEEE, "Design of Low Power, High Speed, Low Offset and Area Efficient Dynamic-Latch Comparator for SAR-ADC ", *in Applied of International Conference on Innovative*

Trends in Communication and Computer Engineering (ITCE), Aswan, Egypt, pp.299-302, (2020).

[23] E. Alnasser, "A Novel Low Output Offset Voltage Charge Amplifier for Piezoelectric Sensors ", *IEEE SENSORS JOURNAL*, VOL. 20, No.10 pp 5360-5367, (2020).

[24] E. Choa, et al, "Radiation Hardened Op-amp Design for 1 Mrad TID ", *Transactions of the Korean Nuclear Society Virtual Spring Meeting*, 2020.

[25] A. Sheeparamatti, et al, "Design of 3.3V Rail To Rai Operational Amplifier for High Resolution ADC] Driver Amplifier", *in Applief of International Conference Innovative Mechanisms for Industry Applications*, pp 317- 320, 2017.

[26] Kavyashree C L, et al, S. MP, "Design and Implementation of two stage CMOS Operational amplifier using 90nm technology", *in Applied of International Conference on Inventive Systems and Control*, pp. 1-4,(2017).

[27] G. Venkatrao, et al," Design of Low Power and High CMRR Two Stage CMOS Operational Amplifier in 180nm Technology" *International Journal of Innovative Research in Science, Engineering and Technology*, Vol. 5, Issue 5,pp. 6746-6752, May (2016).

[28] D. Nageshwarrao, et al, "IMPLEMENTATION AND SIMULATION OF CMOS TWO STAGE OPERATIONAL AMPLIFIER", *International Journal of Advances in Engineering & Technology*, Vol. 5, No. 2, pp. 162-167, (2013).