Design and Simulation of Low Power Wilson Current Mirror and Single Supply CMOS Level Shifter

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Abstract.

The low power Wilson current mirror level shifter and the single supply CMOS level shifter are briefly described in this study. The suggested method examines the drawbacks of the traditional, highly high-power WCMLS. Using CMOS 65nm and 90nm technology, the suggested method produced reduced power consumption. In addition to WCMLS, the design of a single-supply CMOS level shifter employing 65nm and 90nm technology is covered in this study. The main advantage of CMOS level shifters is their low power consumption. The Mentor Graphics tool is used to simulate the WCMLS and Single Supply Level Shifter. When employing 65nm and 90nm, WCMLS uses 14.3nW and 14.7nW of power, respectively, while the voltage level changes from 0.4V to 1.5V using 65nm and 0.4V to 2.5V for 90nm. The amount of power used by a single supply CMOS level shifter using 65nm and 90nm is 10.7nW and 11.5nW whereas voltage level transformed from 1.25V to 2V.

Keywords: Low power consumption, Wilson current mirror, Single supply CMOS level shifter, Mentor Graphics tool, CMOS Technology.

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1 Introduction

In contemporary, largely digital circuits and systems, lowering the supply voltage dramatically decreases both the static and short-circuited power as well [1] as the dynamic power. The circuit's speed is nonetheless constrained by the low supply voltage, which also affects the linearity and inherent gain of the analogue sub threshold blocks. The multiple supply voltage approach, in which each block runs with its own local supply voltage, is being used by new and growing applications. This includes biomedical implants and wireless sensor nodes, which often need medium speeds and low power. The voltage level shifter (LS) links the sub-blocks by mixing several supply voltages. The LS is in charge of increasing low level voltages to values that the next stages can tolerate. The LS should be low power, quick, and have a compact silicon area to minimize system performance effect. Due to the trend of lowering supply voltages below the nominal threshold voltage of MOS transistors, LSs must function at low supply voltages [2].

Due to the daily rise in demand for portable electronics like cell phones, iPods, cameras, etc., system designers pay close attention to the system's low power consumption. Dynamic and static power dispersal [3] are the two types of imperativeness dispersal seen in VLSI circuits. The immediate result of charging and discharging the storage capacitor is dynamic power dispersion

The spilling current that passes through VLSI circuitry causes static power dispersion. Power loss is mostly caused by the supply voltage. As a result, changing the supply voltage may minimize overall power dissipation. Leakage Current, a negligible voltage

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fluctuation [4], and inadequate noise margin are all effects of lower supply voltage.

2 Existing System

Pull-up networks are used in customized and controlled systems to conserve electricity and increase speed. Employing CM-based topologies. WCMLS [5] uses a feedback transistor to stop static current in standby mode. Proposed LS design uses a modified Wilson current mirror to decrease VDDL. As a means of power reduction, a self-regulating current limiter using output defect detection is offered. By getting rid of the input inverter, the work in decreases the falling edge latency. By applying a level-shift capacitor to a voltage differential between VDDH and VDDL that has been repeatedly charged, [4] reduces the falling edge delay.

One supply VDDH is all that is needed for a single supply level shifter to transform a low voltage [5] signal into a higher voltage. VDDH is output. The output voltage is higher than vin. To lower the output voltage, set VDDL.

3 Proposed System

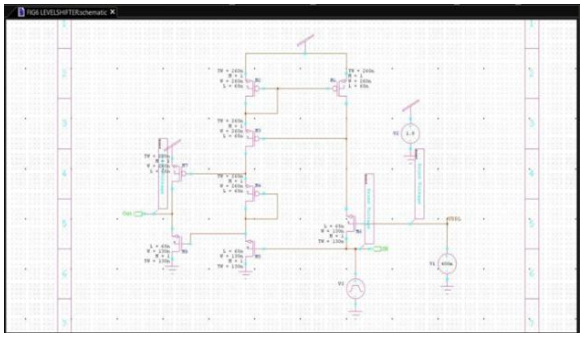

Fig. 1. Modified Wilson current mirror level shifter

The proposed LS's streamlined schematic is shown in Fig. 1.A modified WCMLS structure is used in the design, which can significantly lower energy usage. The static current through the output inverter is significantly reduced because there are fewer output inverters and because node Q1 has a greater voltage swing than node Q2, especially for low values of L3Having fewer output inverters minimizes dynamic current.

Simulation waveforms show that the recommended circuit decreases both dynamic and static current taken from VDDH [6] (i.e. IDDH).The power consumption is further decreased by connecting a p-MOS diode Mp1 in series.

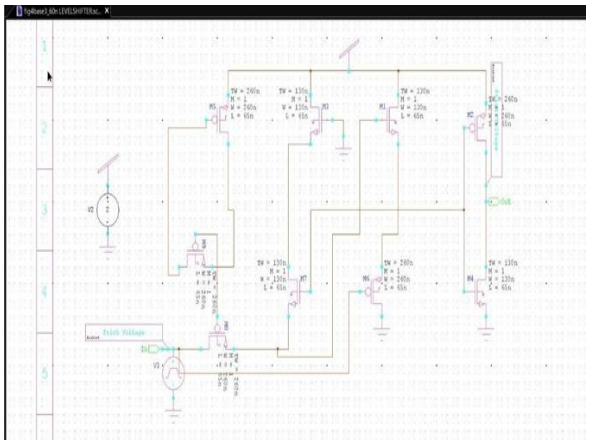

Fig.2. Modified Single supply CMOS level shifter

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Figure 2 shows the revised CMOS level shifter circuit. Low input turns off NMOS Q7 and on PMOS Q6. As a result, Q6 controls VDD and provides an input to Q8 and Q9 gates. Q8 directs the output to ground while Q9 is turned off. Input high turns on NMOS Q7 and off PMOS Q6. Q7 disables Q8, supplying GND to Q8 and Q9's gates. Q9 turns VDD into the output. By making the circuit less complex, the major goal of this circuit is to consume less power [7]. Circuit prioritizes minimal power usage above all else.

4 Results and Discussions

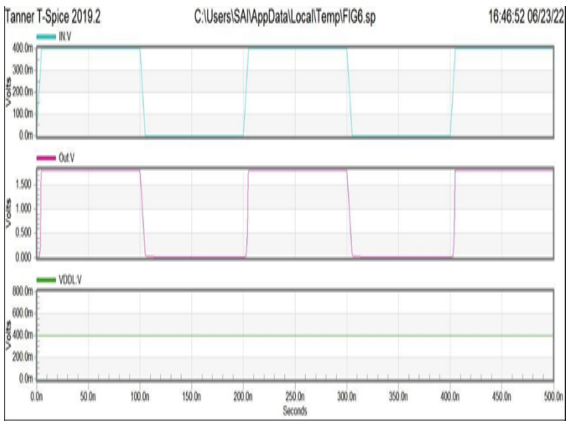

Fig.3. Simulation result Wilson current mirror level shifter with 65nm technology

By simulating the proposed work in a standard 65nm CMOS technology, voltage levels are shifted from 0.4v to 1.8v. The power consumption [8] is reduced drastically and the area also reduced by decreasing transistor count. The power consumption is recorded as 14.3nW for 65nm respectively

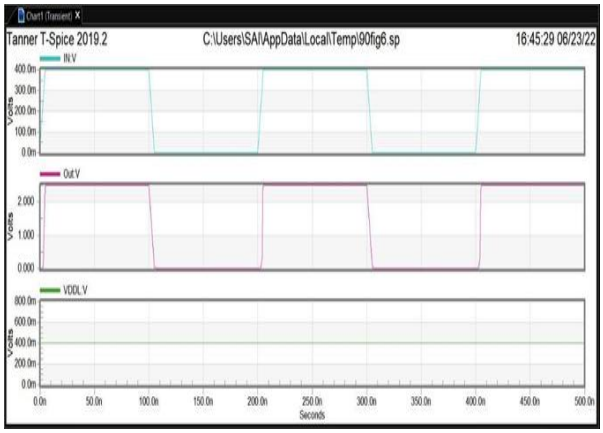

Fig.4. Simulation result Wilson current mirror level shifter with 90nm technology

By simulating the proposed work in a standard 90nm CMOS technology, voltage levels are shifted from 0.4v to 2.5v. The power consumption is reduced drastically and the area also reduced by decreasing transistor count. The power consumption is recorded as 14.7nW for 90nm respectively [9]

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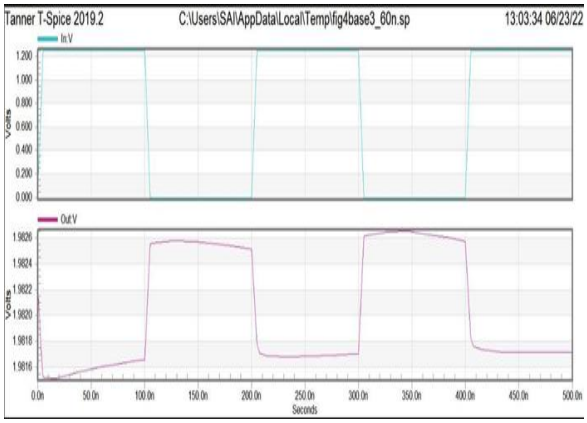

Fig. 5.Simulation result of single supply CMOS level shifter with 65nm technology

The above simulation results show that under 65nm Single supply CMOS level shifter [10] [11], the voltage levels will be transformed from 1.25V to 2V, the power consumption is reduced drastically and the area also reduced by decreasing transistor count. The power consumption [12] is recorded as 10.7nW for 90nm respectively.

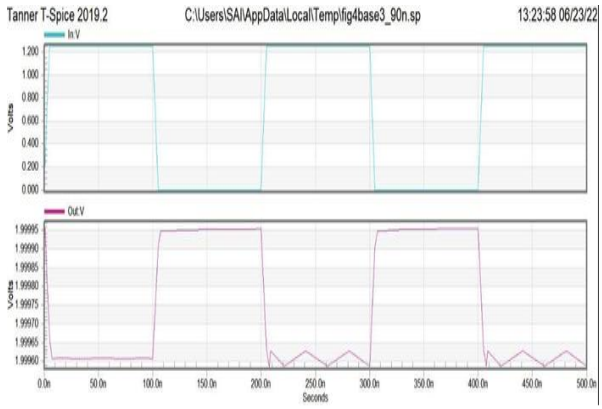

Fig. 6. Simulation result of single supply CMOS level shifter with 90nm technology

The above simulation results show that under 90nm Single supply CMOS level shifter, the voltage levels [13] will be transformed from 1.25V to 2V, the power consumption is reduced drastically [14] and the area also reduced by decreasing transistor count. The power consumption is recorded as 10.7nW for 90nm respectively.

Table 1: Comparison with Prior Works

TECHNIQUES USED	WILSON CURRENT MIRROR LEVEL SHIFTER		SINGLE SUPPLY CMOS LEVEL SHIFTER	
	EXISTING	PROPOSED	EXISTING	PROPOSED
TRANSISTORS USED	11	8	12	9
TECHNOLOGY USED	180nm	65nm,90nm	45nm	65nm,90nm
POWER CONSUMPTION	76.34 nW	65nm-14.3nW 90nm-14.7nW	115.43nW	65nm-10.7nW 90nm-11.8nW

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5 Conclusion

Using 65nm and 90nm technology, three CMOS level shifters and a Wilson current mirror level shifter are built in this research. Comparing the two level changers' power consumption Wilson current mirror level shifters are made with high output impedance, which means they consume less power since they require relatively little current. Because the leakage current is smaller, the single supply CMOS level shifter consumes less power. The single supply CMOS level shifter consumes 10.7 nW while the dual supply CMOS level shifter consumes 11.8 nW. Wilson contemporary mirror level shifters use 14.3nW and 14.7nW of power, respectively. When compared to Wilson current mirror level shifters, single supply CMOS level shifters are shown to use less power.

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