A NOVEL LOW-POWER HIGH-SPEED CMOS COMPARATOR FOR PRECISE APPLICATIONS

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ABSTRACT: The process of converting analogue signals to digital signals widely uses comparators. Comparators are the fundamental components of many types of ADC (Analog to Digital Converters). In order to improve their performance, many structures have been presented. Performance of a comparator is strongly affected by powers, delayed, offsets, and noises. A novel Low-Power High-Speed CMOS (Complementary Metal Oxide Semiconductor) Comparator for Precise Applications is presented in this analysis. The decision stage and hold stage are the two stages that make up this dynamic comparator for Complementary Metal Oxide Semiconductors (CMOS). Three different phases are used to operate the comparator. Which maintains the results of an evaluation for a defined time interval, reset is the initial phase, decision or evaluation is the second phase and hold is the third. Energy efficiency can be increased while overall power usage is decreased. The length of time that the presented comparator is in a low state is important. The 16.1 version of 18nm technology will be used to build this comparator's design, which will result in a significant improvement in power and delay. According to the results, the provided comparator performs better than the NMOS (N-channel Metal Oxide Semiconductor) and PMOS (P-channel Metal Oxide Semiconductor) comparators in terms of power dissipation and time delay.

KEYWORDS: Comparator, Analog to Digital Converters, Complementary Metal Oxide Semiconductor

I. INTRODUCTION

The advancement of CMOS technology is responsible for the advancement of integrated circuits (ICs). Digital signal processing simulations will consequently gain in popularity. Standard components in all ICs that converted an analogue signal into a digital signal are called Analog-to-Digital Converters (ADCs) [1].

The comparator, which compares two analogue inputs and generates digital outputs, is one of the most important blocks in integrated circuits. Voltage comparators have three key architectures: open-loop comparators, regenerative latch comparators, and preamplifier latch comparators [2]. The Comparators are utilized in a wide range of applications, including switching power regulators and data transfer.

The process of converting analogue signals to digital signals widely uses comparators. To start the A/D conversion process, the input must be sampled. To identify the digital equivalent of the analogue signal, this sampled signal is applied to a combination of comparators, which compares the analogue signal to another reference signal and generates a binary signal depending on the comparison. Comparators are the fundamental building blocks in the architecture of ADCs [3].

On high performance VLSI (Very Large Scale Integration) and battery backups systems, a power issues are one of the most significant restrictions. Many analogue circuits, such as high speed analog-to-digital converters (ADCs), memory sense amplifiers, and data receivers, depends on high speed and low power comparators. The comparator in analog-to-digital converters is essential to the overall effectiveness of the converter. Any high resolution and high speed data converter requires a fast and accurate comparator.

With the advent of CMOS technology and the miniaturization of MOS transistor sizes, the capabilities of mixed-mode

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signal circuits for storing and processing large amounts of data have increased are converted to digital representation before being processed. As a result, Analogue-to-Digital Converters (ADCs) are being used more frequently. The demands for high-speed and low-power ADCs is growing as a result of the expansion of mixed-signal circuit usage in numerous systems, including video systems, wireless communications, Ethernet, and healthcare organizations [4]. In the majority of modem telecommunications networks, the main components at the front-end of a radio-frequency receiver are low power and high speed ADCs.

Comparators can be divided broadly into two categories, such as static and dynamic comparators. Dynamic comparators are based on clocks, whereas static comparators are dependent on amplifiers. In generally, dynamic comparators are chosen over static comparators due to their quick turning speed and lack of static power dissipations. On the other hand, the ADC resolution is constrained by the larger voltage offset and kickback noise of dynamic comparators. The comparator is the ADC component that utilizes the most power. As a result, the power consumption of the ADC must be decreased. As a result, a good comparator that is exact and accurate is essential for an amplifier. There is always a tradeoff between size and speed in CMOS devices. Larger transistors are utilized to increase the speed of the comparator and balance the drop in supply voltage, but they consume more power and take up more spaces.

Operating with low supply voltages makes designing high-speed comparators more difficult. In other words, for a specific technology, in order to increase speed, transistors with width and length values are needed, which also increases chip area and power, to make up for the supply voltage reduction. ADCs mostly utilize dynamic comparators because these comparators have high speed, less power dissipation and zero static power. Another application of back-to-back inverters is in dynamic comparators, where they serve as a positive feedback mechanism that transforms a slight voltage differential into an output of a full-scale digital levels. The accuracy of such comparators is controlled by output load capacitance and parasitic node capacitance. A novel, high-speed, low-power CMOS comparator for precise applications is presented to address these issues.

The remaining of the approach is arranged as follows: The related analysis is described in section II. The section III demonstrates a novel, high-speed, low-power CMOS comparator design for precise applications. The section IV demonstrates the result analysis of presented approach. Finally the analysis is concluded in section V.

II. LITERATURE SURVEY

Rama Prasad Acharya, Abir J Mondal and Alak Majumder et. al. [7] describes a method for designing a comparator for applications that sample data in data processing. In this method, an unique comparator architecture with a look-ahead circuits is developed to decrease worst-case delays and enhance performance. To significantly decrease the essential path latency, a multilayer look-ahead circuit is first described. Second, the complexity of the entire architecture is greatly reduced by utilizing domino logic to implement the comparator and multilevel look-ahead circuit. According to simulation results, the presented 64-bit circuit dissipates power more efficiently than existing architectures.

Shilpi Singh et. al. [8] describes a novel CMOS dynamic latch comparator for low power and high speed. This analysis examines a unique dynamic latched comparative that uses less power and operates faster than standard dynamically latching comparators. In terms of power and delay, this analysis provides a comprehensive review of various comparator design types. Using a 1V voltage power supply and 180 nm CMOS

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technologies, Tanner EDA suite was used to design and simulate the transient responses of the comparators and the described circuit.

Shruti Hathwalia et. al. [9] presents Low Power CMOS Comparator Analysis and Design at 90nm Technology. In terms of performances, powers, and delays, this approach gives a comprehensive analysis of a range of comparator systems. The dynamic latch preamplifier employs a fully differential circuit to minimize the impacts of offset voltage error produced due to device imbalance. It is composed of a preamplifier with a double regenerated dynamically latches. A basic dynamic latch comparator is the first stage of a buffered dynamic latch circuit, which is followed by an inverter buffer stage. Large node capacitance is also utilized to reduce offset errors, and inverter buffers are added to isolate the comparator output. Utilizing GPDK (Cadence Generic Process Design Kits) 90nm technology, comparators are created and their transient responses are modeled in the Cadence Virtuoso Analog Design Environment.

Rohit Mongre, R. C. Gurjar et. al. [10] presents a 0.18µm technology, in order to use an ADC, a low-power, high-speed comparators are designed. This method presents a CMOS comparators with a faster speeds and low power consumptions. This comparator's schematic design is implemented in 0.18µm UMC (United Microelectronics Corporation) technology with a 1.8-volt power supply and is cadence Virtuoso-simulated. The simulated outcomes are displayed, and they indicate that this structure is capable of operating at high speeds. Additionally, they used schematic view designs to confirm the current results. They also compared these findings to earlier available work to confirm improvements.

Suman Biswas, Dr. J.K DAS et. al. [11] Analog to digital comparator with ultra low power and high speed is described. Cadence virtuoso analog design environment analyzes the circuits in GPDK 45nm and 180nm technologies. The described comparator is displayed in 180nm, and a comparison between the prior architecture. The proposed architecture uses 56% less power than the existing architecture. The circuit minimizes kickback noise and offsets voltages, which makes the pipelines perfect for flash and data converting applications.

Rangaraju H Ga, Raja K B c, Vinayak Hegdeb, Muralidhara K Nd et. al. [16] design of an efficient reversible binary comparator is presented. The NOT, PG (Power Gate) and CNOT (controlled-NOT) gates are used in the designing of an input circuits and a one-bit comparative cell. The first stage of an n-bit reversible binary comparator is an input circuit, and the second stage is a one-bit comparator cell, and so on. It computes the inputs and outputs of Constant, Delay, and Garbage. When compared to existing techniques, the provided technique has reduced quantum cost and garbage output values.

III. NOVEL LOW POWER HIGH SPEED COMPARATOR

This section introduces a novel low power high speed comparator for precise applications. The CMOS dynamic comparator's structure is illustrated in Figure 1. The two stages of this dynamic comparator are as follows. There is a hold phase and a decision phase.

The operation of a comparators are divided into three stages. Reset is the initial phase, decision or evaluation is the second, and hold is the third, which stores stored the evaluation results for a specified period of times. Transistors M7 and M8 are on when clk1 is high during in the reset phase, whereas M9 and M10 are off. As a result, through nodes M7 and M8, nodes Vi-n and Vi-p are shorted to grounds. The selection phase (evaluation) starts when clk1 is lower. In this phase, the node voltages Vo-n and Vo-p are raised by the input signals Vi-n and Vi-p. In consideration of the V_{IP}

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– V_{REF} + and V_{IN} – V_{REF}- signal levels, the output voltages V_{OUT}+ and V_{OUT}- will have different speeds.

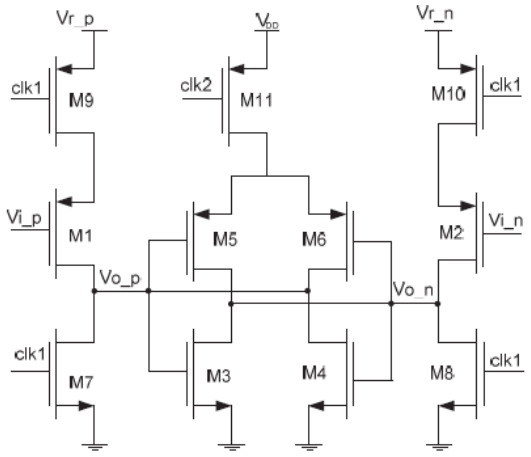

Fig. 1: CMOS Dynamic Comparator

One voltage approaches the NMOS transistor's threshold voltage and is connected to Vdd earlier by two cross-coupled inverters. The other voltage is connected to ground. As a result, Vdd or Gnd are connected to one of the Vo-p and Vo-n. If the output nodes really aren't restored for more comparisons, input signals fluctuations cannot alter the output level after this phase (the evaluation time). In this architecture, the duration of the clock pulse clk2 can be used to manage the inputs offsets.

In this structure, the hold phase requires power consumption for CMOS inverters but is where power is removed. The first stage contains power dissipation, then by changing the structure, the hold phase's power consumption can be decreased. A current will be pulled from Vr-p under the assumption that the output node Vo-p equals Vdd following the evaluation phase. In Fig. 2, the current path is shown. Transistors M1, M4, and M9 are on in this path. There is no requirement for this current during the hold phase. Two solutions to this issue are proposed with this description of the comparator's operation.

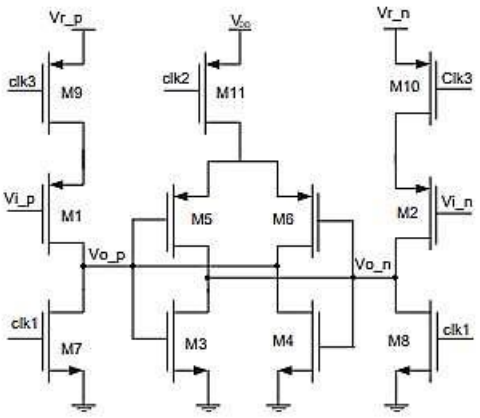

Fig. 2: Presented CMOS Comparator

This is based on the concept of triggering the M9 and M10 transistors with a different clock pulse. Along with clk1, it goes low, but after establishing the latch's condition, it restores to high. In this situation, M9 and M10 are off, and neither current nor power is received from Vr-n or Vr-p in during evaluation stage.

The kickback noise that is produced at the latch during the decision phase is reduced due to this separation. I_{IN}+ and I_{IN}- are produced as a result of the voltages differences in between inputs branches as well as the references divergences voltages. This action occurs during the amplification phase. The cross coupled inverter's regenerative loop increases the differential voltage during the third phase.

Decision Point**:** With regard to the reference differential voltage V_{REF} diff, a comparator evaluates the inputs are the differential voltages. First, grounded is used to discharge the output nodes Vout+ and Vout-. As soon as the clock strikes, an amplifications begins. Clk1 decreases while Clk2 maintains a high value. The input transistors M5 and M6 are resistively connected to the linear region in which the transistors M7 and M8 function. At the start of the third stage, the outputs nodes starting voltages are Vout+=I_{IN}+ tamp/CL, Vout-=I_{IN}-tamp/CL. The sign of the Vout+ and Vout- determines which direction the comparator swings once it has reached the third phase. Vin+-V_{REF}+ and V_{IN}-V_{REF}- are

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responsible for controlling the input current.

IV. RESULT ANALYSIS

This phase uses the Tanner tool with the 16.1 version of 18 nm technology to construct a novel Low Power, High Speed Comparator for Precise Applications. This section explores the evaluation of presented scheme using experimental results. Figure 3 illustrates the waveform of an NMOS two-stage dynamic comparator. Clk and Clkbar are set to "1" and "0," respectively, in the initial phase known as the reset phase. The comparator's first and second phases are respectively reset to GND (Ground) and VDD (Positive Supply Voltage) when, the evaluation phase begins by changing the values of clk and clkbar to '0' and '1', respectively.

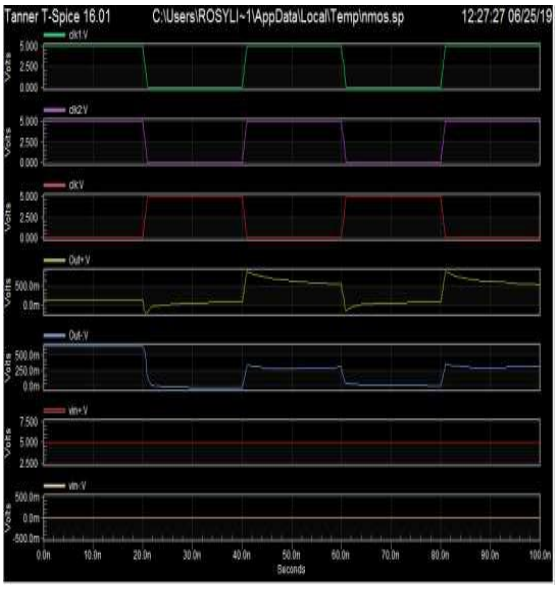

Fig. 3: Output Wave Form of NMOS Two-Stage Dynamic Comparator

During this evaluation stage, the input differential signal (Vin+ -Vin) of the NMOS transistor is utilized to differentially charges the parasite capacitors at the preamplifier's output nodes. As soon as the latch is activated, its input differentially voltage develops until the rail-to-rail differential signal is produced. For fast amplification, the latch uses a positive feedback circuit. In same condition, as shown in Figure 3, the preamplifier's output voltages are charged to VDD.

In order to discharges the output voltages of the preamplifier and latches to GND during resets, the restart phases of clk, clkb1 and clkb2 are all logic '1'. toggled clk and clkb1 to logic '0' enables pre-amplification during the evaluation process. Now, the cross-coupled circuits improve the differences voltages while decreasing the common mode voltages. The NMOS two-stage dynamic comparators can have the optimum delay because to the inherently effective elimination of the issue by the PMOS comparator. Therefore as outcome, it improves speed while consuming reduced power. The Fig. 4 shows the output waveform of PMOS two stage dynamic comparator.

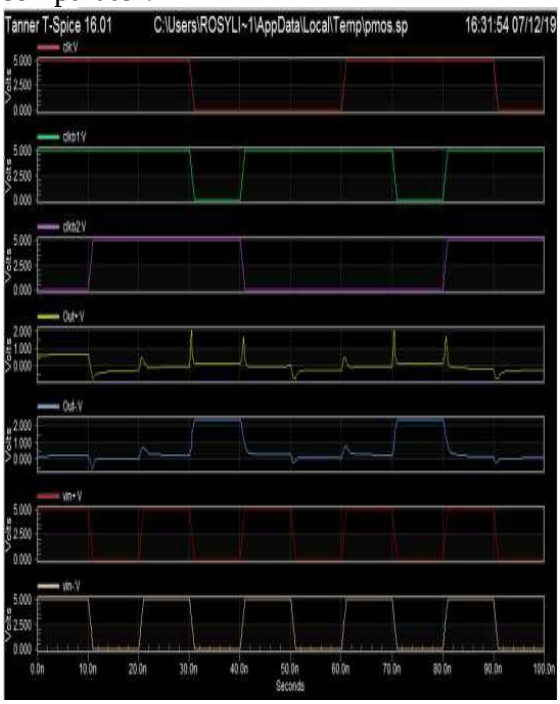

Fig. 4: Output Wave Form of PMOS Two-Stage Dynamic Comparator

When clk3 is low, power is lost in the CMOS comparator, but no power is lost during reset and evaluation. When compared to the NMOS and PMOS two-stage dynamic comparators, the overall power consumption is reduced and energy efficiency can be increased. The M9 and M10 transistors are activated by another

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clock pulse, which is the basis of the CMOS. It goes low simultaneously with clk1, but once the latch's condition is determined, it goes high once again. This condition leads in M9 and M10 being off, no current being drawn from Vr-n and Vr-p, and no power being sacrificed during the evaluation phase.The table 1 shows the comparison between earlier and presented approach.

Table 1: Performance Comparison

Comparator Type	Total Nodes	Delay (s)	Power (mW)
NMOS	28	1.73	0.011
PMOS	35	1.63	0.015
CMOS	26	0.83	0.02

The table 1 shows the comparison of area, delay and power for different transistors. Combining the NMOS and PMOS transistors leads in a change in the presented CMOS comparator, which allows the area, delay, and power to be compared for CMOS comparator. The Fig. 5 shows the output waveform of presented CMOS comparator.

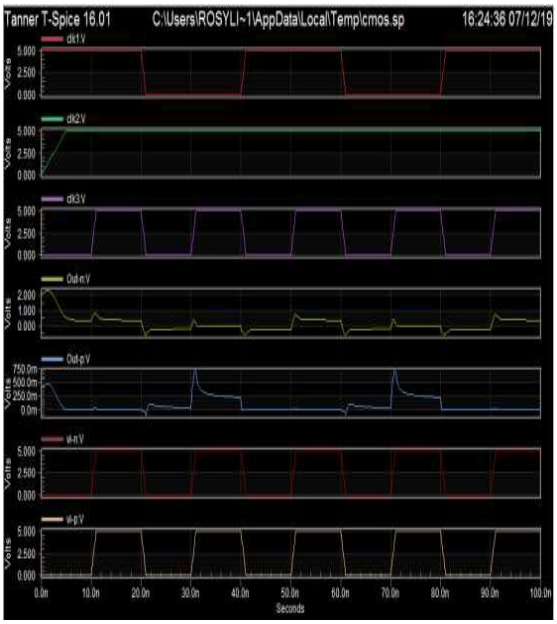

Fig. 5: Output Wave Form of Presented CMOS Comparator

V. CONCLUSION

This analysis utilized Tanner EDA tool with 16.1 version of 18 nm technology to create a novel low power and high speed CMOS comparator for precision applications. Increasing the delay and power demonstrates a CMOS dynamic comparator region with low power, high speed, and low offsets voltages. The presented circuit, which combines the two latches into a single circuit, uses CMOS comparators to lower power consumption and improve speed. The simulation shows that the CMOS comparator is better in delay and power consumption than the NMOS and PMOS dynamic comparators. In future work, the performance of the CMOS dynamic comparator may be improved in its speed, delay and power consumption by using gain boosting technique for data converter circuits and in advanced medical equipment embedded with the sensors.

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