Choice and control Interleaved boost converter for multi-stack fuel cell applications.

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ABSTRACT.

Today, Fuel Cell Electric Vehicles (FCEV) have substantial challenges regarding reliability and control. Multi-Stack fuel cell (MSFC) technology provides an innovative method for tackling some of these issues, particularly reliability. This paper reviews the literature on electrical association architecture studies on MSFCs with converters. An analytical study has also been presented to choose the optimum association architecture and the best suitable boost converter topology promising in FCEV applications regarding lower input current ripple, reduced inductance size, improved efficiency and higher reliability. According to the findings, the interleaved boost converter (IBC) topology and parallel association architecture of each fuel cell with a converter is the best choice for such applications.A control strategy of an FC stack using a non-isolated 4-Phases DC/DC boost converter has been presented and validated. This control is ensured by hybrid duel loop control, including voltage and rapid current loops with linear PI controllers. The simulation results demonstrated the converter's and control strategy's high efficiency and functionality.

Key words:*FC Current ripples, FCEV , FIBC, Interleaved DC/DC Boost Converter, Multi-Stack Fuel cell,PEMFC ,Reliability.*

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1. INTRODUCTION.

Much research on clean vehicles is now being undertaken [1].FCEVs can provide a solution because they do not contribute to local pollution [2]. The Fuel Cell (FC) combines hydrogen and oxygen to create power, heat, and water with no pollution emissions, making it a clean generator [3, 4].

The Proton Exchange Membrane Fuel Cell (PEMFC) is one of the most promising existing FC technologies for power generation in automotive applications [5, 6] because of its relatively small size, solid electrolyte, and high efficiency [7-9]. Moreover, this type of FC operates at relatively low temperatures, around 80°C. Therefore, the low-temperature operation allows them to start up quickly (i.e. less run time preheating) and results in less thermal stress on system components, allowing for better durability [10]. Generally, FC systems must meet severe technical requirements regarding operating temperature, energy efficiency, weight/volume and reliability [11]. Once all these conditions are met, the FC market will undoubtedly be encouraged and contribute to moving from a very small industry to mass production.

One way to improve at least some of these requirements is to consider MSFC architectures, where these architectures can improve efficiency, reliability and cost [12-14]. The architecture design of MSFC must be optimized as a whole rather than individually optimizing each specific subsystem. In this perspective, the FC and its output converter must be designed to create a so-called optimizing power module. Thus, this leads to meeting the following three requirements of a win-win integration, namely:

1. Thermal compatibility between the FC and the converter.
2. A compact converter by improving energy efficiency and increasing switching frequency.
3. An extended thermal capacity of the "FC/converter" module to cover harsh environments.

This paper discusses the various electrical association of MSFC structures with converters offered in the literature and identifies the benefits and drawbacks of these associations to select the best MSFC association architectures. Then, two non-isolated Interleaved Boost Converters are distinguished, which have many advantages that make them strong candidates for use in FCEV, followed by an in-depth study from the standpoint of minimizing the input current ripple, size of the inductors, and improving the efficiency and reliability of these converters in the various studied association architectures. Finally, a hybrid dual-loop control strategy for the selected converter is also presented in this paper.

Different electrical architectures of MSFC combinations.

Various couplings of FCs via DC-DC converters can be envisaged, which can be used as an energy source for transport applications. These combinations have different advantages and disadvantages, which are presented in the following subsections.

1.1. MSFC association by a single converter

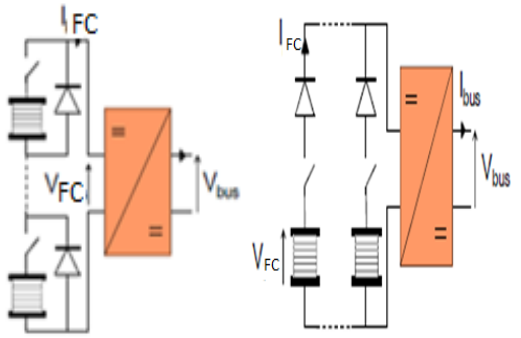
A first so-called "natural" association solution for FCs consists of connecting them either in series or in parallel with a single converter

FCs in series:

Figure 1(a) shows that a single converter connects the MSFC to the DC bus. This architecture uses a low-gain converter that generates less stress on the converter switches. However, it has a flaw in that the breakdown of one or more FC generators may cause the system to shut down [15]. Thus, in such a structure, adding a by-pass circuit to each FC is recommended to isolate the faulty stack and ensure the circulation of the current and the delivery of a percentage of the total power [16]. Admittedly, this electrical association is characterized by its ease of implementation, but when a fault occurs in the converter, it leads to the complete shutdown of the system.

FCs in parallel:

The FCs are in series with a switch and a diode (Figure 1(b)). The role of the switch is to disconnect the faulty stack. Since an FC is not a reversible system, a diode is present to prevent reverse currents. A disadvantage of this combination is the difficulty in controlling the power supplied by the FCs. This combination requires a high boost ratio converter.



(a) (b)

Figure 1. MSFC with single converter: (a) in series, (b) in parallel

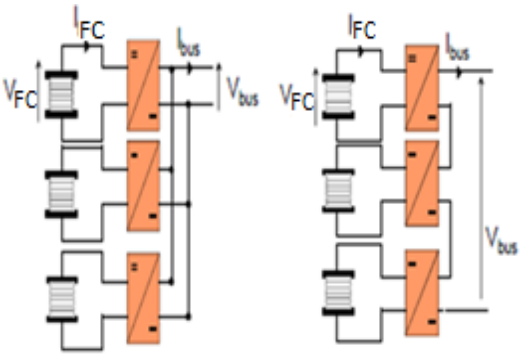
1.2. Association each FC by a converter

Parallel architecture:

Figure 2(a) shows that each FC stack is connected to the DC bus through a converter. This architecture ensures redundancy and individual control of each FC and allows the system to operate in degraded modes. This architecture uses a high-gain voltage converter, resulting in higher power switch stress [17].

Cascade Architecture:

This association, as shown in Figure 2(b), allows power to be shared between different FCs [18]. The overall DC output voltage is distributed among the different FCs, and this architecture uses only low-voltage converters, which are less stressful on the power switches. However, there is difficulty in controlling and adjusting the output voltage of this combination



(a) (b)

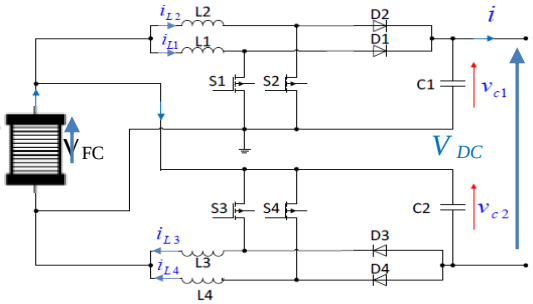
Figure 2. Each FC with converter: (a) in parallel, (b) in Cascade

3. Choice of MSFC association architectures and DC/DC converters interface.

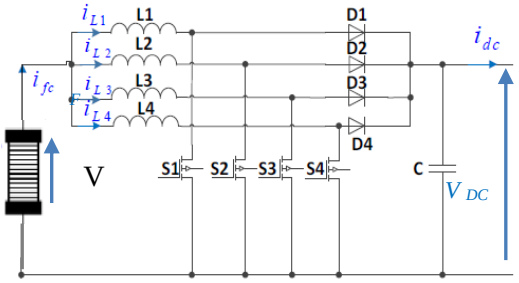
In order to define which topology is best suited for different association architects via DC-DC converters and to choose the most appropriate topology and association architectures for our application, two non-isolated DC/DC converter topologies will be highlighted which candidates are for use in FCEV. The comparison between these two topologies is made in the different association architectures via DC-DC converters from the viewpoint of minimizing input current ripple, values of inductors, efficiency energy and reliability.

3.1. Interleaved DC/DC converter topologies

Interleaved topologies are very suitable for cycle efficiency improvement [19, 20]. Several articles have highlighted the advantages of this topology compared with other converter's topologies for FC applications [21, 22]. In particular, Floating Interleaved Boost Converter (FIBC) and IBC topologies are the most attractive converters due to their ability to manage the high FC current by appropriate sharing between the phases, supply power to the load in case of power switch fault, reduce FC current ripple and electrical stress applied to semiconductor devices [23, 24]. In this study, the two topologies will be used in 4 phases. The architecture of the 4-Phase FIBC is given in Figure 3(a), while the architecture of the 4-Ph IBC is given in Figure 3(b).



(a)



(b)

Figure 3. the two Interleaved topologies.
(a) 4-Ph FIBC (b) 4-Ph IBC

Structurally, the two converters are similar except for the two-part segmented DC link capacitor for the first (C1 and C2 in Figure 3(a)). The interleaved input branches are placed in parallel, while the DC link capacitors are connected in series.

3.2. Comparison between the two topologies in each Association Architecture

As mentioned above, the comparison that will be discussed below will be made from the viewpoint of input current ripple reduction, inductance volume, reliability, and power efficiency. In this study, three stacks FC with the characteristics indicated in Table 1, which show the characteristics of the studied system, will be used

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Table 1. Systems specifications

Parameters	Variable
PEMFC rated power, P_{FC}	21 KW
PEMFC rated voltage, V_{FC}	70 V
PEMFC rated current, I_{FC}	300 A
DC Bus voltage, V_{dc}	360 V
Switching frequency, F_s	10 KHz
Inductor, L	130 µH
Capacitor, C	495 µF

3.2.1. FC current ripple (Δi_{FC})

The influence of high FC current ripple has been studied in the literature. Studies have shown that increases in the FC current ripple have a greater impact on life, efficiency, and hydrogen consumption and lead to much greater deterioration, especially on the lifetime of platinum catalysts [25, 26]. In the literature [27, 28], it has been suggested to limit the current ripple to less than 10% of the rated FC current. In the following, a comparison between the two converters will be made to evaluate the best topology for reducing the

ΔiFC in each FC association architecture via the converter. The expressions for the ΔiFC for the two topologies are given by:

$$\Delta i_{FC} = \begin{cases} \frac{Vdc(1-4D)D}{L.f} for\ 0 < D < 1/4 \\ \frac{Vdc(4D-1)(2-4D)}{4L.f} for\ 1/4 < D < 1/2 \\ \frac{Vdc(4D-3)(2-4D)}{4L.f} for\ 1/2 < D < 3/4 \\ \frac{Vdc(4D-3)(1-D)}{L.f} for\ 3/4 < D < 1 \end{cases} \quad (1)$$

Where D is the duty cycle, V_{dc} is the DC bus voltage, f is the switching frequency, and finally, Δi_{FC} is the FC current ripple.

To calculate the $\Delta i_{FC}$for the two topologies in each architecture association. First, the duty cycle of each converter must be determined, which is determined from the voltage ratio (V_{dc}/V_e) of each converter and is given in the following relations:

$$D_{IBC} = \frac{\frac{V_{dc}}{V_e} - 1}{\frac{V_{dc}}{V_e}} \quad (2)$$

$$D_{FIBC} = \frac{\frac{V_{dc}}{V_e} - 1}{\frac{V_{dc}}{V_e} + 1} \quad (3)$$

For the two cases of association in series (Figures 1(a) and 2 (b)), the values of the duty cycle (D) are 0.41 for the IBC topology and 0.26 for the FIBC topology, and for the two cases of association in parallel (, Figures 1(b) and 2(a)), the values of the duty cycle are 0.8 for the IBC and 0.67 for the FIBC.

In order to compare the ΔiFC of the two topologies, the inductance value of each topology is calculated from the above (1) relationship, taking into account the duty cycle values of each topology.

In the case of series association, the value of ΔiFC of the IBC is approximately five times greater than that of the FIBC, while in the case of association in parallel, we obtain that the ΔiFC of the FIBC topology is approximately one and a half times greater than the ΔiFC of the IBC topology.

3.2.2. Inductance value

Reducing both the value of the inductor and the current through it leads to a reduction in the size, weight and cost of the inductor. The value of the inductors for each topology will be determined in the following by considering that the input current ripple does not exceed 4% of the rated current of the FC used in this study, where these values are determined by the use of the expression (1) above. The values of the inductances for each topology are indicated in the tables of the components selected for each FC association architecture in the sub-paragraphs below.

3.2.3. Converter Reliability

As mentioned earlier, interleaved topologies have several advantages. One of which is reliability, as they have the ability to be fault tolerant naturally, allowing the remaining healthy phases to be used as a compensation system in the event of a switch fault occurrence in each phase, thereby avoiding consequently any interruption in the supply of energy to the load. Both "4-Ph IBC and 4-Ph FIBC" have fault tolerance, but the latter has less freedom in that it must operate with an even number of phases. This constraint limits its ability to operate in degraded mode. By comparison, the 4-Ph IBC is fault tolerant even with a single phase, which makes it a more suitable candidate for working in degraded mode.

3.2.3. Energy efficiency

Each interleaved boost DC/DC converter topology shown in Figure 3 is analyzed to evaluate the losses in each component, which helps to determine the most suitable topology in terms of optimizing energy efficiency in each architecture of the FCs association.

3.2.3.1 The energy losses and efficiencies of the converters in each association architecture.

In the following, the losses in the two converters that we are going to calculate can be divided into two parts: the losses in the inductors and in the semiconductor components. Capacitance losses that are primarily attributable to equivalent series resistances are not considered.

As mentioned above, decreasing the current in each phase in both converters provides more flexibility in the semiconductors and reduces the size of the inductors. However, these components can be subjected to more constraints, in particular, in a degraded mode of operation in the event of the loss of one or more phases. Therefore, the semiconductors have been sized to ensure the reliability of the two converters in the event of a two-phase fault (i.e. when the 4-Ph IBC becomes to 2-Ph IBC and the 4-Ph FIBC becomes to 2-Ph FIBC). The values of the

inductors are determined so that the Δ*i*FC ratio does not exceed 4% of the FC current rating. As we mentioned above, 3 FCs will be used in this study with the characteristics shown in Table 1 above.

a) **Each FC with a converter**

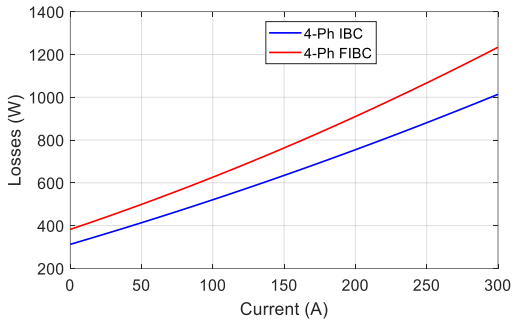
- Parallel Associations

In this association architecture, the input voltage (V_e) of the converters is equal to 70 V , and the output voltage (V_{out}) of each converter is equal to 360 V. The chosen components are defined in Table 2 below.

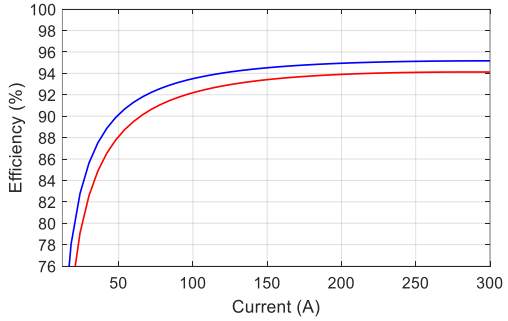
Table 2. converters components (parallel association)

Converter	Switch	Diode	inductance
4Ph-IBC	IGBT (IXGN400N60B3)	Fast recovery(DSEK300-06A)	L_x=120µH (AMCC50)
4Ph-FIBC	IGBT (IXGK400N30A3)	Fast recovery (DSEC240-04A)	L_x=163 µH (AMCC63)

Figures 4 give the evolution of the losses and the energy efficiencies of each structure according to the input current in this association architecture.



(a)



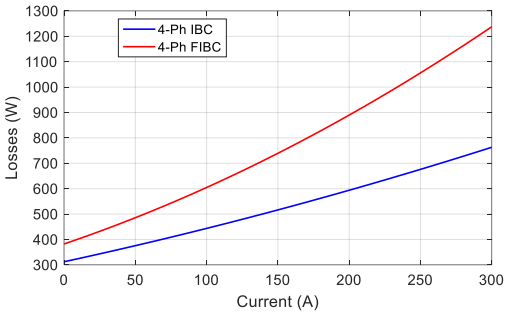
(b)

Figure 4: losses and efficiency of the converters in parallel (a) losses, (b) efficiency

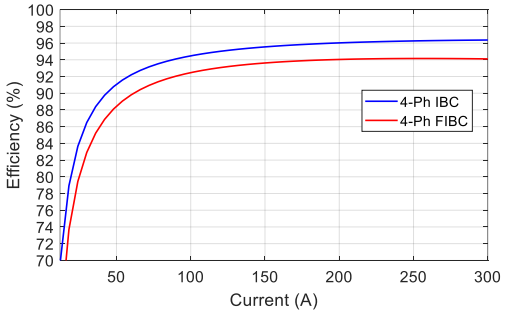
As can be seen from Figure 4 (a), the losses of the 4-Ph FIBC are slightly higher than the 4-Ph IBC, where the difference increases as the current increases. Thus, as shown in Figure 4(b), the overall efficiency of this association architecture with the use of the IBC converter is better than when using the FIBC.

- Cascade associations

In this association (Figure 2(b)), the voltage ratio is low because the V_{out} of each converter is 120 V, which allows a reduction in the value and size of the inductors and a reduction in the stress of the semiconductors, but these inductors and semiconductors must be chosen taking into account operation in degraded mode. Accordingly, the components of the converters will be the same as those shown in Table 2 above. The losses and efficiency of this association in each converter are shown in Figure 5.



(a)



(b)

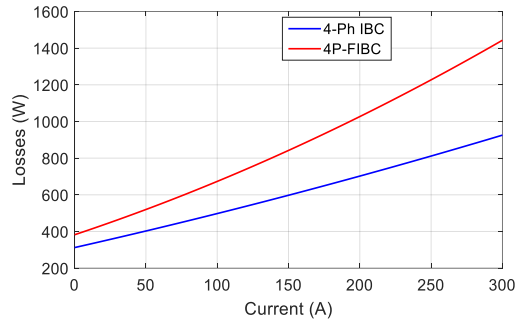
Figure 5: losses and efficiency of the converters in cascade (a) losses, (b) efficiency

According to these correlation curves, we can also observe that the 4-Ph IBC has fewer losses than the 4-Ph FIBC (Figure.5 (a)). Furthermore, as compared to the parallel association illustrated in Figure 4 above, smaller losses were recorded in the 4-Ph IBC, but the losses in the 4-Ph FIBC remained almost the same. As shown in Figure 5(b), the energy efficiency of this association's IBC structure is greater than that of the FIBC structure.

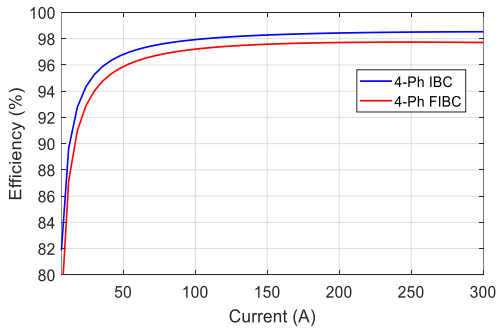
b) **One converter for MSFC:**

- MSFC in series with a converter

In this case, and when the three FCs operate, the Ve is the sum of the voltage of each FC and is equal to 210 V, and the Vout is equal to 360 V. Consequently, the duty cycle is low, which makes it possible to reduce the size of the inductors. But considering the degraded mode, the inductors and semiconductors that should be used in this case are the same when combining a single FC with a converter, and they are the same components shown in Table 2 above, so the loss in this converter will be the same as in the case of an association each FC with a converter in parallel when only one FC operate in this series association. But this loss can decrease when all the FCs operated at their rated output.



(a)



(b)

Figure 6: losses and efficiency of the MSFC in series with a converter (a) losses, (b) efficiency

As shown in Figure 6(a), the losses of the FIBC increase compared to the two cases association above, while the losses of the IBC are limited between the two previous association cases. However, from figure 6(b), an increase in the efficiency of the two converters has been obtained due to the presence of a single converter in this association architecture. Furthermore, the efficiency of 4-Ph IBC is also better than that of 4-Ph FIBC, even in this combination.

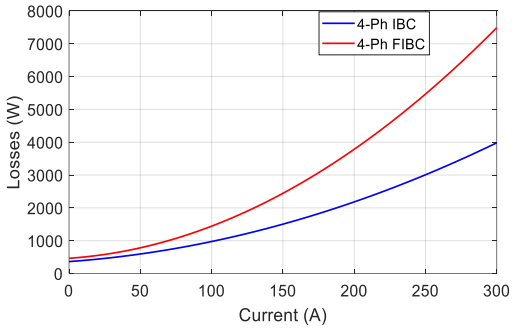
- MSFC in parallel with a converter

Here, the V_e of the converter is 70 V, and the V_{out} is equal to 360 V, but the input current is the sum of the current of each FC, the latter leading to the use of high current semiconductors, which leads to significant losses. The components used are given in Table 3 below.

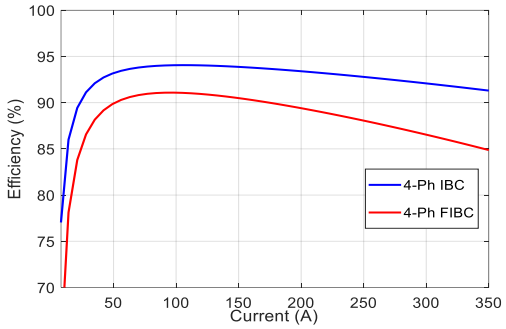
Table 3. converters components of Multi-Fc in parallel

Converter	Switch	Diode	inductance
4Ph-IBC	IGBT (MG06600WB-BN)	Fast recovery(F1000LC080)	L_x=120µH (AMCC50)
4Ph-FIBC	IGBT (MG06600WB-BN)	Fast recovery (F1000LC080)	L_x=163 µH (AMCC63)

The evolution of losses and energy efficiency for each converter is shown in Figure 7.



(a)



(b)

Figure 7: losses and efficiency of the MSFC in parallel with a converter (a) losses, (b) efficiency

By analyzing the above curves, it can be observed that the losses in the FIBC structure when the converter is operating at full power are close to double those obtained with the IBC structure (Figure 7(a)); hence the latter structure has the best performance in this association architect. However, as stated earlier and illustrated in Figure 7, the losses in this association are very high, making it unsuitable for automotive applications.

4. ANALYSIS AND DISCUSSION

According to the obtained comparison results, we conclude that the IBC structure has better energy efficiency than the FIBC structure in all the studied associations. In addition, we recorded the low inductance value of this converter (4-Ph IBC) and its high reliability.

In terms of association architectures selection, the best energy efficiency of the studied association was recorded in the MSFC in series with a single converter. The energy efficiency of this association exceeds 98%, which is a good percentage in automotive applications. In fact, although this association is less expensive and simple to control than the architectures association of each FC with a converter, it has certain disadvantages which affect the FC life, especially when reconnecting a faulty recoverable FC. Hard restart (coupling the FC to the system by closing its corresponding switch Sn during operation) could lead to current peaks that would damage the recovered FC [29]. In addition, this architecture is considered less reliable since many FCs are connected to a single converter, which can cause a complete shutdown of the system when a fault occurs in the converter. It is recommended to use the association architectures of each FC with a converter To avoid a sudden restart; These associations make it possible to control each FC independently, which increases the degrees of freedom and offers a greater adaptation to operation in degraded mode.

On the other hand, during the comparison in terms of energy efficiency between the two association architectures of each FC with a converter, we see that there is a very slight difference between the two architectures when using the 4-Ph IBC. We can therefore choose the parallel association because the cascade association is more expensive since a capacitor is used for each converter, while only one capacitor common to all converters can be used in parallel association. Also, the control of the cascaded architecture can be complex and less stable compared to the parallel architecture. In addition, this recently mentioned architecture is more reliable and does not require additional components when operating in degraded mode. Furthermore, as mentioned earlier, the Δ*i*FC value and inductance size of the IBC topology in this latter architecture (parallel) is lower than the FIBC topology.

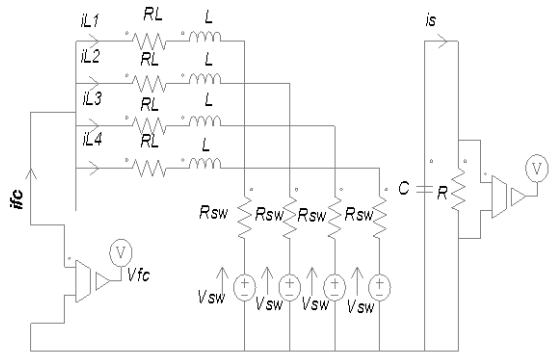
In conclusion, both from the point of view of energy efficiency, input current ripple, inductor size and reliability. The IBC topology and the parallel association of each FC with a converter are the best choices for this study.

5. Modeling and control of the 4-Ph IBC

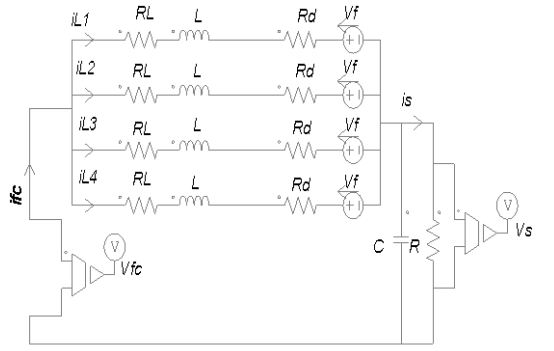
5.1. Modeling of the converter

In order to design the controls of the chosen converter and for performance purposes, appropriate dynamic models are required. There are several types of electrical modelling of converters; These types of modelling can be classified in decreasing complexity as follows: instantaneous models, average models, and finally, “small average signal” models [30]. For our work, we opted for the “Average in small signals” model because it is the most widely used, according to the literature.

Figure 8 represents the equivalent electrical diagrams of the 4-Ph IBC according to the two operating periods (i.e. for 0<t<DTs and DTs<t<T).



(a)



(b)

Figure 8: electrical equivalent diagram of 4-Ph IBC: (a) 0<t<DTs, (b) DTs<t<Ts.

Where *RL* represents the parasitic resistance of the inductance L.

- In the on the state: each power switch is equivalent to an internal resistance (R_{sw}) and the threshold voltage (V_{sw}), each diode is

equivalent to an internal resistance (R_d) and the threshold voltage (V_f)

- The resistance of each non-conductive switch or diode is infinite. First, the converter equations are given for the two operating periods shown (0<t<DTs and DTs<t<T). To simplify the analysis, we only take into account the parasitic resistance of the inductance *RL*. For the sequence of operation (0<t<DT), the equations are given below:

$$\begin{cases} L\frac{di_{L1}}{dt}(t)=V_{fc}(t)-R_L i_{L1}(t) \\ L\frac{di_{L2}}{dt}(t)=V_{fc}(t)-R_L i_{L2}(t) \\ L\frac{di_{L3}}{dt}(t)=V_{fc}(t)-R_L i_{L3}(t) \\ L\frac{di_{L4}}{dt}(t)=V_{fc}(t)-R_L i_{L4}(t) \\ C\frac{dV_s(t)}{dt}=-i_s(t) \end{cases} \quad (4)$$

For the sequence of operation (DTs<t<Ts), the equations are given below:

$$\begin{cases} L\frac{di_{L1}}{dt}(t)=V_{fc}(t)-R_L i_{L1}(t)-V_s(t) \\ L\frac{di_{L2}}{dt}(t)=V_{fc}(t)-R_L i_{L2}(t)-V_s(t) \\ L\frac{di_{L3}}{dt}(t)=V_{fc}(t)-R_L i_{L3}(t)-V_s(t) \\ L\frac{di_{L4}}{dt}(t)=V_{fc}(t)-R_L i_{L4}(t)-V_s(t) \\ C\frac{dV_s(t)}{dt}=i_{L1}(t)+i_{L2}(t)+i_{L3}(t)+i_{L4}(t)-i_s(t) \end{cases} \quad (5)$$

Subsequently, the average modelling was applied to equations (4) and (5) above. The average converter model studied is given below:

$$\begin{cases} L\frac{di_{L1}}{dt}(t)=V_{fc}(t)-R_L i_{L1}(t)-(1-D1)V_s(t) \\ L\frac{di_{L2}}{dt}(t)=V_{fc}(t)-R_L i_{L2}(t)-(1-D2)V_s(t) \\ L\frac{di_{L3}}{dt}(t)=V_{fc}(t)-R_L i_{L3}(t)-(1-D3)V_s(t) \\ L\frac{di_{L4}}{dt}(t)=V_{fc}(t)-R_L i_{L4}(t)-(1-D4)V_s(t) \\ C\frac{dV_s(t)}{dt}=(1-D1)i_{L1}(t)+(1-D2)i_{L2}(t)+(1-D3)i_{L3}(t) \\ \qquad +(1-D4)i_{L4}(t)-i_s(t) \end{cases} \quad (6)$$

The dynamic model of small signals of the studied IBC is obtained as:

$$\begin{cases} L\frac{d\tilde{i}_{L1}}{dt}(t)=\tilde{V}_{fc}(t)-R_L\tilde{i}_{L1}(t)-(1-D1)\tilde{V}_s(t)+V_s\tilde{d}_1(t) \\ L\frac{d\tilde{i}_{L2}}{dt}(t)=\tilde{V}_{fc}(t)-R_L\tilde{i}_{L2}(t)-(1-D2)\tilde{V}_s(t)+V_s\tilde{d}_2(t) \\ L\frac{d\tilde{i}_{L3}}{dt}(t)=\tilde{V}_{fc}(t)-R_L\tilde{i}_{L3}(t)-(1-D1)\tilde{V}_s(t)+V_s\tilde{d}_3(t) \\ L\frac{d\tilde{i}_{L4}}{dt}(t)=\tilde{V}_{fc}(t)-R_L\tilde{i}_{L4}(t)-(1-D1)\tilde{V}_s(t)+V_s\tilde{d}_4(t) \\ C\frac{d\tilde{V}_s(t)}{dt}=(1-D1)\tilde{i}_{L1}(t)-i_{L1}\tilde{d}_1(t)+(1-D2)\tilde{i}_{L2}(t) \\ \qquad -i_{L2}\tilde{d}_2(t)+(1-D3)\tilde{i}_{L3}(t)-i_{L3}\tilde{d}_3(t) \\ \qquad +(1-D4)\tilde{i}_{L4}(t)-i_{L4}\tilde{d}_4(t)-\tilde{i}_s(t) \end{cases} \quad (7)$$

Assuming that the duty cycles (D1, D2, D3 and D4) are identical, the transfer functions in the Laplace domain of this converter are given below:

- The output voltage / duty cycle:

$$G_{vd}(S)=\frac{\tilde{V}_s(s)}{\tilde{d}(s)}=K_{vd}\frac{(1+\frac{S}{w_{zI}})}{(\frac{S}{w_n})^2+\frac{S}{Qw_n}+1} \quad (8)$$

- The inductance current / duty cycle:

$$G_{id}(S)=\frac{\tilde{i}_L(s)}{\tilde{d}(s)}=K_{id}\frac{(1+\frac{S}{w_z})}{(\frac{S}{w_n})^2+\frac{S}{Qw_n}+1} \quad (9)$$

- Output Voltage / Inductor Current:

$$G_{vi}(S)=\frac{\tilde{V}_s(S)}{\tilde{i}_L(s)}=\frac{K_{vd}(1-S/w_{zI})}{K_{id}\ (1+S/w_z)} \quad (10)$$

With :

$$K_{vd}=\frac{V_s}{(1-D)}\left(\frac{4R(1-D)^2-R_L}{4R(1-D)^2+R_L}\right)\cong\frac{V_s}{(1-D)} \quad (1)$$

$$w_{zI}=\frac{4R(1-D)-R_L}{L} \quad (12)$$

$$w_n=\frac{1}{\sqrt{LC}}\sqrt{\frac{4R(1-D)^2+R_L}{R}} \quad (13)$$

$$Q=1/2\xi \quad (14)$$

$$\xi=w_n\frac{L+RR_LC}{2(R_L+R(1-D)^2)} \quad (15)$$

$$K_{id}=\frac{2V_s}{2R(1-D)^2+R_L} \quad (2)$$

$$w_z=\frac{2}{RC} \quad (3)$$

The transfer functions (8) and (9) are second-order systems with two cut-off pulsation poles (13), and with a zero (12), (17). The cut-off frequency and also the zeros are a function of the duty cycle D. In a closed loop system, the elements of the system will change when the duty cycle changes, which means the transfer function also changes. This makes the controller design for this converter much more challenging from a stability and bandwidth perspective.

5.2. Converter control strategy

The optimal design of a corrector is a difficult task because the parameters of the transfer function strongly vary with the load R. In order to select the correctors and to design them correctly, it is important to define control objectives [31] , which can be formulated as follows:

- The V_{out} of the converter must be regulated at all times in the event of load variations and operating conditions of the FC affecting the polarization curve.
- The input current of this converter must be distributed evenly over the different phases of the converter in order to avoid an overload in one of the phases, especially with high load values. Additionally, the phase currents must be properly offset from each other to minimize input current ripple, which is undesirable in FC applications [31, 32].

- Ensure stability and dynamic performance when the system is running in a closed loop.

- Control with two loops:

The converter connected with an FC suffers from input voltage variation and load current change. Therefore, to regulate a constant output voltage to better power the load, a dual loop controller shown in Figure 9 is required. The external loop voltage controller generates the total reference current (ifc_{ref}) for the internal loops by processing the reference voltage and the measured voltage. This reference current is then divided equally between the phases of the converter to obtain the reference current (iL_{ref}). Then the inner loops produce the duty cycles Di (i = 1, 2, 3, 4). Accordingly, the duty cycle signal is sent to the pulse width modulation (PWM) block to produce the ON-OFF signals for controlling the power switches (S1, S2, S3, S4). It should be noted that usually, the carriers in four PWM blocks are phase shifted uniformly by Ts/4 in order to reduce the input current ripple.

Linear proportional regulators of type proportional integrator (PI) are used in both loops. Figure 9 shows the control block diagram integrating the two closed-loop control loops.

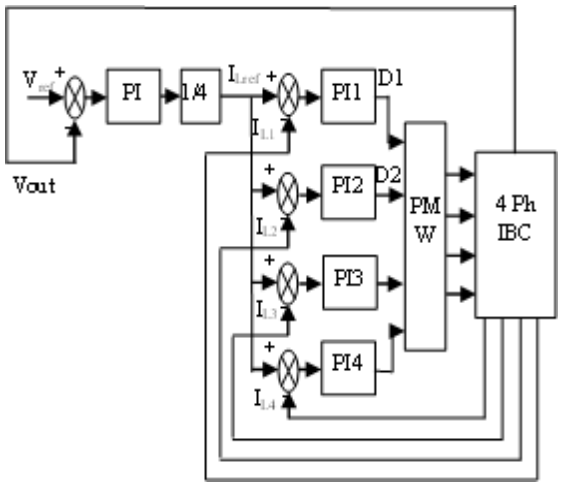


Figure 9: Control structure with two control loops.

The parameters of the regulators PI (of the two loops) are calculated using the graphical poles-placement of the transfer functions$G_{vi}(S)$ and $G_{id}(S)$underMatlab's SISO-Tool.

The parameters of these regulators have been optimized to meet design requirements such as gain margin (MG), phase margin (MP) and settling time.The PI regulator transfer function is of the following form:

$$PI = \mathrm{Kp}(1 + \frac{1}{\mathrm{TiS}}) \qquad (4)$$

The parameters of these PI regulators of the two loops are:

- Externalloop:Kp= 4 et T_i= 0.05.
- Internal loops:Kp= 0.04 et T_i= 0.005

5.3. Simulation results

The FC stack and the used converter had been simulated under the Matlab-Simulink Software, Table. 1 above shows the parameters associated with the system.

Figure 11 depicts the output voltages' behaviour during a positive step load change. As illustrated in Figure. 10, the load changes from 6 to 7 ohms. It is obvious that the IBC voltage tracks its reference well, demonstrating that the converter's controller exhibits outstanding dynamic performance over the load cycle with acceptable overshoots due to load fluctuations.

The following results are shown in the Figures. 12 and 13 show the behaviour of the inductors' and FC's currents. They arrived swiftly at their references, which are given by PI regulators. Consequently, the PI controller gives excellent tracking and a short response time.

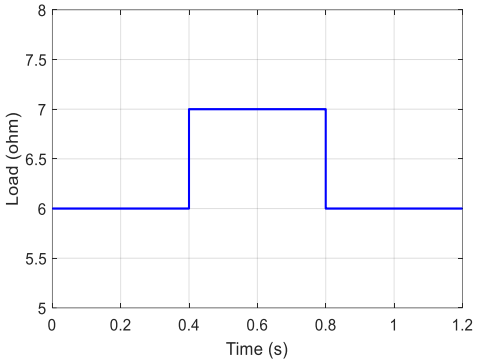


Figure 10: Load cycle.

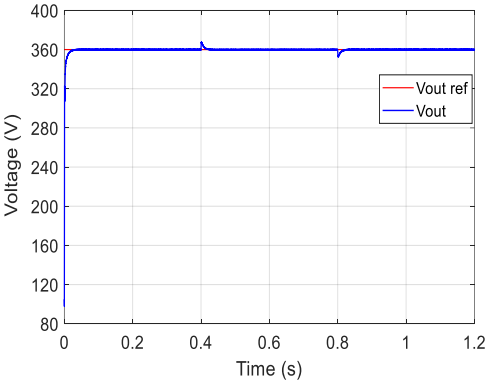


Figure 11: 4-Ph IBC output voltage V_{out}

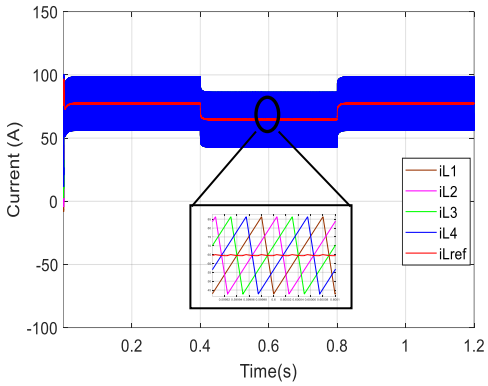


Figure 12: Inductors current and its reference.

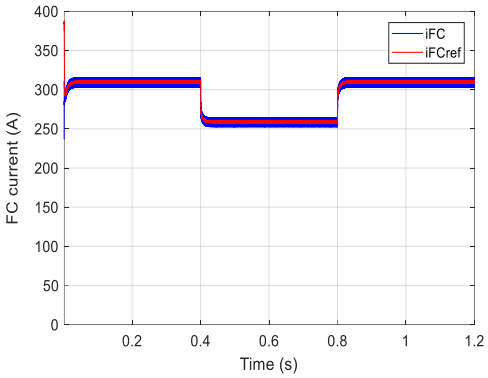


Figure 13: Fc current and its reference.

CONCLUSION

An analytical study is carried out in this paper to determine the most suitable electrical association architecture for the MSFC proposed in the literature, as well as the most suitable power converters in this architecture, whereby a comparison is made between two non-isolated Interleaved DC/DC Boost Converters (IBC) in different association architecture, in terms of minimizing size Inductors, reduce FC current ripple, improve efficiency and high reliability. The parallel architecture of the MSFC association with each converter and the IBC topology was adopted after examining the outcomes of this study. This paper also proposes a control strategy for the converter chosen from the results of this analytical study. The obtained results show the efficiency and good functionality of the converter and control strategy.

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