DESIGN OF IMPROVED DISTRIBUTED CANNY EDGE DETECTION ALGORITHM (IDCEDA) AND ITS VLSI IMPLEMENTATIONS

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ABSTRACT

Recently Automatic Image Segmentation and edge detection techniques have become more popular and commonly used in many applications like Road Sign Detection in ADAS systems, Medical Image Diagnosis Machine vision systems etc. Generally, information about the object is available at the edges or boundaries and high frequency noise or an artifact exists in the boundaries due to improper image acquisition process. Hence, it is very difficult to interpret or process such type of images. In this paper we proposed improved distributed canny edge detection algorithm (IDCEDA) to segment or detection of the object boundaries into more accurate and it is synthesized ISE environment the final layout is developed through TSMC 0.18um technology. The proposed design gives more accurate results with minimum no. of hardware resources compared to existing approaches in terms of accuracy and less hardware resources required for implantation. The proposed algorithm performs superior than the existing approaches in terms of Hardware Resources Utilized and sharp edge boundaries of images. Finally, the algorithm is implemented on vertex family of FPGA devices for effective estimation of Real time performance of the proposed algorithm.

Keywords: Edge Detection, Image Segmentation, De-noise, FPGA, VLSI Architecture
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I. INTRODUCTION

Now a day's all hospitals are employed digital technologies to enhance the benefits of patient health diagnosis process. Medical image quality assessment, disease diagnosis, localization of object boundaries is a fundamental task of the doctor. In fact, from the recent literature many patients have been died because of improper diagnosis of the disease. Basically edges have important message of the object. Over the decades several Researchers have been investigated different solutions to solve noise problems at the image edges. The common approach of all these methods almost same. That is first noisy image is to be smoothed or filtered by suitable filtering approach. Second, is to use first order (or second order) derivative methods for finding local maxima information. Canny Proposed three phase Edge detection method: good detection, good localization and low spurious response. In edge detection Scale of edge detection filter major role. Selection of small scaled filters is very sensitive to noise otherwise selection of large scale filters will remove the fine details of the image. Edge detection is a basic tool in image processing in order to process further computer vision applications like intelligent transportation, automatic machine inspection, driver less automobiles, intelligent robot control systems. The outcome of any edge detection method is

to recognize or locate the edges of different objects. Recognition and classification of images are basically done through the object edge information. Human eye can easily perform this task but machine can't perform this task without edge information. The main drawback of first generation gradient operators like Sobel, Robert and Prewitt is that it cannot work on weak edges results in poor performance in the presence of noise. The advancement of gradient operators are compass operators[1] it can detect more edges with better accuracy but these are computationally expensive. Morphological operators[2] enabled for edge detection and image segmentation. These morphological operators run on sequential processors and it cannot meet real time requirements[3]. The advantage of morphological based edge detection algorithms are not sensitive to noise, easily implement on parallel processing, but it suffers from edge flatness. Later wavelet transformation based methods[4] attracted by many researchers to solve edge detection problems. Fuzzy based edge detection[5] methods are purely based on mathematics and is difficult to implement on hardware, it is complex process. The processing of applying edge detection algorithm for noisy images is tedious job. Since both noise and edge contains high frequency content to attempt to reduce the noise leads to blurred and distorted edges will results. Recently Parallelism and pipelining will enhance the performance of Field Programmable Gate Arrays (FPGAs). Especially for Image Processing applications to access large data from memories, Optimization of system architecture and processing elements will added another advantage. The organization of the paper is as follows section.

The organization of this document is as follows. Section 1 and 2 gives some brief description about the problem and various methods. Section 3 and 4 specifies growth, architecture of FPGA followed by VLSI design process. Some of the recent works are described in section 5. Section 6 gives information about the proposed Algorithm. Finally, experimental results ended by conclusion is described in section 7 and 8 respectively.

II. CONCEPT OF IMAGE SEGMENTATION

The widely investigated field of image processing, image analysis and important module of early vision problems is image segmentation. Image segmentation is the process of separating image into disjoint or distinct regions whose characteristic such as intensity; color, texture etc are similar. Image segmentation is a fundamental part of the low level aspects of computer vision and has many practical applications such as in medical imaging, industry automation and satellite imagery. Traditional methods of image segmentation have approached the problem either from localization in class space using region information, or from localization in position, using edge or boundary information. Segmentation algorithms for monochrome images generally are based on one of two basic properties of gray values: discontinuity and similarity. In the first category, the approach is to partition an image based on abrupt changes in the gray level. The principal areas of interest within this category are detection of isolated points and detection of lines and edges in an image. The principal approaches in the first category are based on edge direction, and boundary detection. Basically, the idea underlying most edge detection techniques is the computation of a local derivative operator. The first derivative of the graylevel profile is positive at the leading edge of a transition, negative at the trailing edge, and zero in areas of constant gray level. Hence the magnitude of the first derivative can be used to detect the presence of an edge in an image. In digital image segmentation, input image is submitted to preprocessing phase, where image enhancement (pre-Processing) operation is carried out by morphological transformation. The result of preprocessing phase is submitted to segmentation phase, where actual segmentation operation is made after it will submitted to post processing and output image is in segmented form.

2.1 Segmentation Techniques

Image segmentation algorithms broadly grouped into following categories:

Thresholding or image binarization is one of the most important approaches to image segmentation. Gray level histogram corresponds to an image f(x,y) composed of light objects on a dark background. One way to extract the objects from background is to select a threshold T that separates foreground and background. At any point (x,y) for which f(x,y)>T is called an object point otherwise it is background point. Thresholding segmentation may not support all types of images at various contrast, uneven background, ridge break etc. The global threshold can be identified by an optimization strategy aiming at creating "large" connected regions and at reducing the number of small-sized regions, called artifacts. The most frequent way is to determine the threshold is based on image intensity histograms. But this approach is very sensitive to noise and no visible histogram valley point's .A group of connected pixels with similar properties is called regions. In this approach first select seed pixel and add some adjacent pixels until to form a region. The absolute intensity range between candidate pixel and seed pixel lie within specified range. The main limitations of region based segmentation approach are that all pixels must be assigned to regions, region must be uniform and any merged pair of adjacent regions must be non-uniform. Unlike region growing, which starts from a set of seed points, region splitting starts with the whole image as a single region and subdivides it into subsidiary regions recursively while a condition of homogeneity is not satisfied? Region merging is the opposite of splitting, and works as a way of avoiding over segmentation. Organizing data into classes such that: High intra-class similarity and Low inter-class similarity. Finding the class labels and the number of classes directly from the data (as opposed to classification tasks).

III. FPGA ARCHTECTURE

Field Programmable Gate Array (FPGA) is a general purpose programmable device that can be programmed by end user for different applications as per requirement unlike traditional Application Specific IC (ASIC). The main important aspect of FPGA can be easily reprogrammed after deployment into a system. FPGA can be programmed by downloading bit-stream into on chip random access memory. FPGA Provides configurable resources used to implement high level arithmetic and logic functions. The resources include dedicated DSP blocks, MAC units, dual port memories, LUTs, registers, tri-state buffers and multiplexers. It provides high parallelism, distributed memory architecture and high cock rates i.e. 500 MHZ, hence it is suitable for wide range of applications. Apart from the advantages FPGA's can also have some drawbacks such as it consumes more power and more area for its programmable part than ASIC. Finally FPGA's and ASIC can provide various solutions for the designer and carefully evaluated before selecting the device. Fig.1. gives the future metrics of FPGAs for various Applications. This graph can be taken as reference for predicting the importance of FPGA and its internal architectural blocks shown in Fig.2. The implementation of image processing algorithms on FPGA is a three step process[6].first, knowing the complete description about both algorithm and software implementation. Second, design should be optimized with respect algorithm (e.g. using transformation techniques) and hardware part (e.g. using more advanced fixed point blocks). Finally we evaluate the complete design for performance parameters like speed, resource utilization, image quality and reliability of the algorithm.

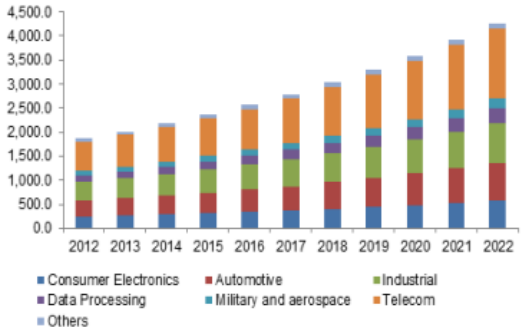

Figure 1. The expected growth of Field Programmable Gate Arrays for various applications

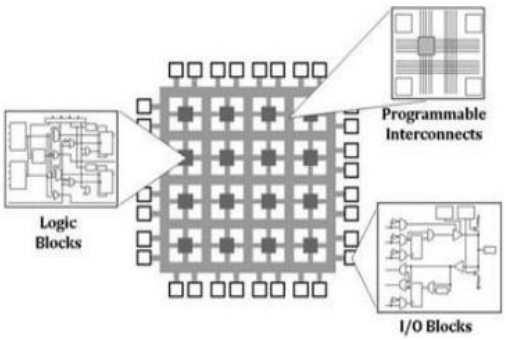

Figure 2. Architecture and its internal blocks of FPGA

IV. RELATED WORKS

Edge detection is one of the fundamental needs in image processing, machine vision and computer vision, medical image segmentation and 3D image reconstruction. Generally, edge has detected according to some early brought forward algorithms such as gradient-based algorithms[7] and template-based algorithms[8] , but they are not so good for noisy medical image edge detection. In order to overcome this problem, adaptive threshold using ACO has proposed. Canny edge detection algorithm used mostly real world edge detection problems because of its superior detection and good localization performance [9] unfortunately, this algorithm requires lot of computational complexity than other edge detection gradient operators like Robert, Prewitt and Sobel. The first edge detection filter with sobel operator proposed in [10]. Filter design here is performed with sobel coefficients i.e. input image is convolved with 3x3 sobel filter mask coefficients to measure the image intensity level along the directions like vertical, horizontal, left and right. These four measurements are combined to estimate magnitude and direction. Finally authors have designed chip for the same and produced edge information. The limitation of this approach is not considered the image diagonal information and not implemented any parallel processing to optimize the hardware. Later [11] proposed New Edge detection Algorithm with absolute difference mask VLSI based architecture by incorporating edge strength unit, parallelism and pipelining. This approach can be detected weak edges and gives single pixel information, finally the overall CMOS based VLSI architecture can execute 30 frames per sec at clock rate of 10MHz. In sobel edge detection [12] authors incorporated edge detection and smoothing operators in parallel to achieve better segmentation results and to improve the speed of operation flip-flop to be considered. Adaptive neural network algorithm [13] finds the one of the feasible solution for image edge detection through this approach authors have found the relationship between momentum factor and error gradient. The accuracy of the detected edges will depends on the adjustment of moment factor values. Normally to divide image into two regions image with the help of binarization process [14], authors have selected adaptive Neural Networks. Low cost VLSI architecture proposed in [15] this approach detected 60% of Impulse noise in images with only two line buffers and fixed window size. The reconstructed image is again given to canny edge detector to validate the results. In [16] authors have investigated different filtering approaches finally proposed fast filtering approach to reduce the high frequency noise and enhance image edge features. In [17] proposed efficient MRI image edge detection method using STICT-FCI incorporated with canny edge detection algorithm. In their view first STICT algorithm applied to improve the quality of source image. Secondly, they are dividing the image into homogeneous regions by using fuzzy C-means clustering technique and finally canny edge detection algorithm was applied to detect the edge information. Though the approach is good in terms of edge detection but it suffers from low PSNR values. Recently fuzzy logic systems commonly employed for solving image segmentation problems. Traditional intensity based fuzzy-c means algorithms can be effectively used to segment the noise free images. Though it fails if the image contains noise and other artifacts. Later fuzzy algorithms along with spatial information were employed for segmentation but this approach is quit complex and requires large memory to update and storing the membership coefficients and centroid mapping. In order to solve large memory size problems [18] proposed three step process: pre-computation, updating the membership

coefficients and finally centroid calculation and up-dation. More recently novel method for solving medical image segmentation using ACM have proposed [19].In their work authors have contributed work for solving in homogeneity problems in brain MRI images.

Comparative metrics

The performance of any segmentation algorithm can be easily evaluated by different evaluation techniques. No unique algorithm for all images and applications. Based on type of image dataset and application the segmentation algorithm will varies. From literature performance evaluation methods are typically classified into subjective type, supervised and unsupervised. In subjective evaluation, humans can visualize the results for each segmentation algorithm and compares manually but it is tedious job. Later supervised evaluation methods came into existence in this type of evaluation segmented image is compared against the reference image. In unsupervised methods produce better results before the evaluation time and that to it is customize the algorithm parameters for better accurate detection.

V. VLSI IMAGE PROCESSING DESIGN

The latest advancements of semiconductor technology leads to powerful reconfigurable FPGA based programmable logic devices it consists of custom hardware, in-built parallelism and dedicated multiply accumulate units. Hence FPGAs are more favorable prototype devices for fast implementation of image processing algorithms. In order to interpret or extract required information of images, to implement advanced image processing algorithms with large data real time systems have imperative [20].

A. Architectural Over view

Hardware architectures for the pre-processing stage and segmentation stage are discussed for a FPGA implementation. Initially, image is processed by the pre-processing module and then the pre-processed image is given to the segmentation module. Block diagram of hardware implementation is show in Figure 3. The original image is loaded in the external memory for processing. Image pixels (top left to bottom right) are stored in the external memory at subsequent addresses (starting address to end address). Stream cache modules are used for read and write operations with the external memory and image processing module (pre-processing or segmentation). Stream cache, pre-processing and segmentation module are discussed in detail in following sections.

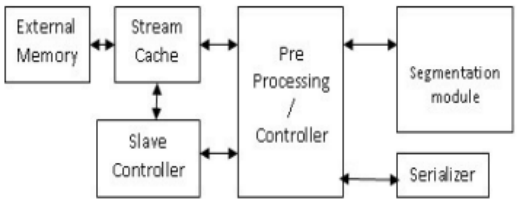

Figure 3. Block diagram of proposed algorithm

Stream cache module is used to make image data communications with the external memory. The input gray scale image is given to pre-processing module from the external memory. The pre-processing module gets one new pixel on every clock cycle from the external memory, processes it and writes back a processed pixel to the external memory. Pre-processing module is designed using a pipeline concept in such a way that it processes a new pixel on each clock cycle. This module has components like serializer, 3 x 3 moving window module, median filter, morphological gradient, thresholding and Serial-In-Parallel-Out (SIPO) shift register module. Flow of the input data and controller signals from one module. Pre-processing module is designed to process only single gray image pixel (8 bit) per clock cycle, serializer is needed to serialize the data. It loads 32 bit data in one clock cycle and provides same data as a stream of four 8 bit data in four clock cycles (one clock cycle for one 8 bit data). In 32 bit data, eight most significant bits (MSB) are part of the first pixel. Eight bits are shifted left on each clock cycle, and a new pixel is shifted to the MSB position and taken as an output data. Each output of the median filter or morphological gradient is a function of nine pixel values within the 3 x 3 window neighborhood. Nine pixels are necessary to read for each window position if caching is not used, and each pixel is needed to read nine times during the image scanning.

B. Basic canny Edge Detection Method

In this section we provide the overview of canny edge detection algorithm [cite] and its implementation details. The total algorithm is represented in different phases: In first phase, the gradient of the each pixel along both x and y direction is to be calculated and is represented as ( ) and ( ) In second phase, after evaluation of ( ) ( ) the magnitude and direction at each pixel.

The magnitude can be evaluated as follows

$$mag(x,y) = \sqrt{f_x(x,y)^2 + f_y(x,y)^2} \text{ ----- (2)}$$

The direction of intensity variation along each pixel

$$ang(x,y) = Tan^{-1}\frac{f_y(x,y}{f_x(x,y)} \text{ ----- (3)}$$

In third phase, the blurred edges are converted into sharp edges by preserving maxima gradient information and suppressing local minima. In this phase use some of quantization techniques along different directions with some fixed angle at each pixel. Final phase is ended by using some threshold methods for preserving noise image edges.

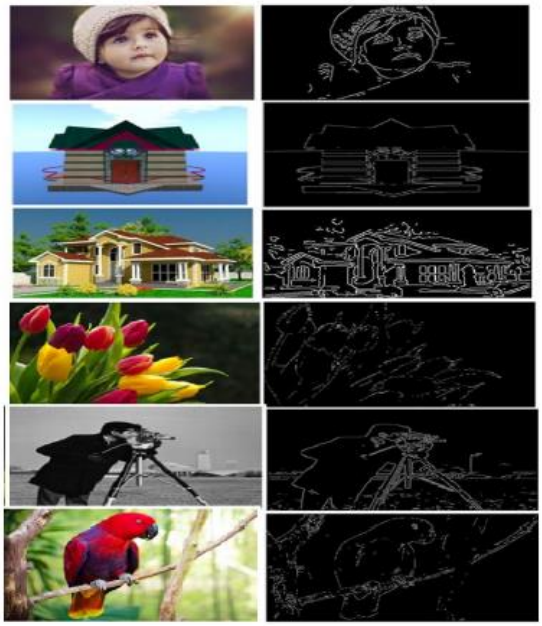

Figure 5. Edge detection of sampled images

VI. PROPOSED ALGORORITHM

The latest advancements of semiconductor technology leads to powerful reconfigurable FPGA based programmable logic devices it consists of custom hardware, in-built parallelism and dedicated multiply accumulator units. Hence FPGAs are more favorable prototype devices for fast implementation of image processing algorithms. In order to interpret or extract required information from images, to implement advanced image processing algorithms with large data real time systems have imperative.

A. Architectural Overview In this paper we proposed improved distributed canny edge detection algorithm (IDCEDA) to segment or detection of the object boundaries into more accurate. In earlier approaches, the lack of threshold detection to compensate the noisy effects in boundaries of the image. In proposed IDCEDA model is represented into seven stages as shown in fig.4. In our proposed algorithm the effects of noise have compensate by subthresold level.

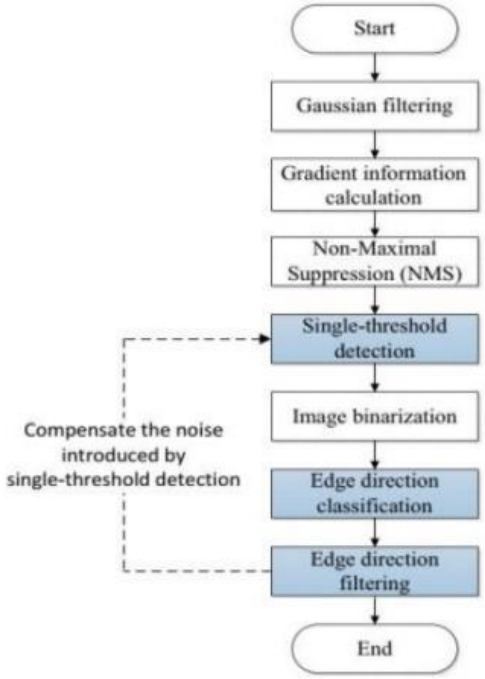

Figure 4. Architecture of proposed IDCEDA Algorithm

Step1: Filter the any noise in the original image before trying to detect and locate edge information. Gaussian mask is applied to smoothen the filtered image. Optimum width of the Gaussian Mask results will give low edge localization error.

Step2: After Eliminating the noise and smoothing process edge strength will increased by applying gradient operators to find the edge strength information.

Step3: Edge direction is computed by taking above gradient information into consideration.
Step4: Maximum suppression has to be applied and it is used to trace edge boundaries.
Step5: Finally, hysteresis method is used to eliminate the image streaking.
Hardware architectures for the pre-processing stage and segmentation stage are discussed for a FPGA implementation. Initially, image is processed by the pre-processing module and then given to segmentation module. The original image was loaded in to external memory for processing, image pixels (top left to bottom right) are stored in the external memory at subsequent addresses. Stream cache modules are used for read and write operations with the external memory and image processing module.

VII. RESULTS AND DISSCUSSION

In this section, we show the efficiency our proposed algorithm in comparison with the basic canny edge detection and distributed canny edge detection algorithms. In our proposed algorithm, we also incorporate adaptive threshold levels for noise detection and edge enhancement approaches. For the evaluation of our algorithm, we take both monochrome and color images. By this method, image edges can easily distinguished shown in fig.5. At the end of the process sub threshold have incorporated to separate the noise from the pixels. For realization of hardware module the complete algorithm is coded in Verilog HDL description language and simulation is carried out using Xilinx Integrated Synthesis Environment tool. Later, the design is implemented on Vertex-5 family of FPGA board the RTL schematic as shown in fig .6. For estimation of accurate boundary detection, hardware utilization the proposed algorithm TMSC 0.18 um CMOS Technology will help us to produce the final layout shown in figure 7.

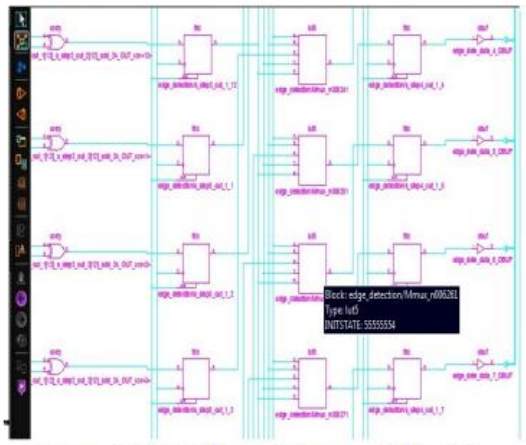

Figure 6. RTL View of Proposed Algorithm

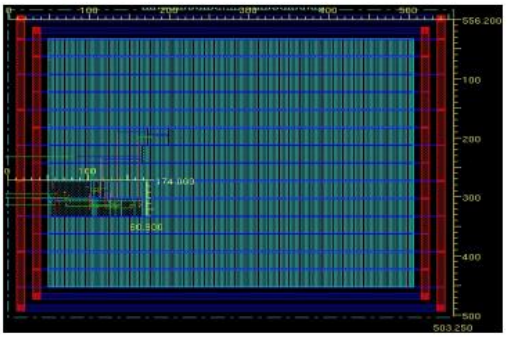

Figure 7. Final Layout of Proposed Algorithm Using TMSC 0.18 um CMOS Process.

VIII. CONCLUSION

The main objective of this paper is to design VLSI based segmentation architecture for implementation on FPGA that gives good segmentation quality, requires less no. of hardware resources with short execution time and is more reliable for real time applications. Preprocessing stage is required to overcome the over segmentation problems. Pipelined architectures are developed for solving delay in execution time. The overall architecture is designed in HDL environment and is synthesized for Xilinx vertex pro FPGA. Different images are tested for segmentation quality and execution time. The proposed VLSI segmentation architecture produced more visually accepted results compared to existing one in terms of less hardware resources and low complexity.

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