



IMPLEMENTATION OF 16 BIT POWER EFFICIENT CARRY SELECT ADDER

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Abstract:

New Technology is quantum dot cellular automata at Nano metric scale, which has lower area (PLBs) requirement and low Power Consumption, quantum cells. by using the CMOS technology, layout size can't lesser than their present size, the QCA approach proves to one of the potential arrangements in beating this physical layout. Using this QCA technology, we created Majority gate, with the help of the Majority gate calculations, new Binary coded Decimal (BCD) adder has developed. The method is simulated and synthesized using Xilinx ISE software with the help of Verilog programming language. The results shown that the proposed method has better performance properties like delay (speed), power utilization, area, ADP and PDP compared to existing methods.

Keywords: QCA, CMOS, BCD

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1. INTRODUCTION

represent the two binary digits, "1" and "0". In Any VLSI design aims at optimization of any simplest form QCA is four dot nano cell composed of three parameters namely power, area and delay. of four dots at corner of the square. The fig.1 given Many researchers have achieved this optimization below represents a QCA cell. The four dots of using CMOS technology. CMOS technology gives quantum cell represents holes and electrons. White very promising results and if we try to extend the colored dots represent holes and black colored dots same CMOS technology to nanometer range there represent electrons. Thus, there are four dots in length and width of the channel becomes too small QCA quantum cell out of which two are filled with and hence transistor loses its functionality. A electrons and two are filled with holes and now if alternative CMOS in nanometer scale a new we apply charge, the two electrons are free to technology QCA (Quantum Cellular Automata) has occupy any hole and thus we can have two different been developed. QCA is one of the promising combinations of holes and electrons in as illustrated technologies that have been employed in modern in fig.1. These two different combinations of holes VLSI design for optimization of power and area. The and electrons are used to represent the two stable crucial feature of a QCA cell is that it possesses an states binary 0 and binary 1 in QCA technology. electric quadrupole which has two stable orientations. These two orientations are used to



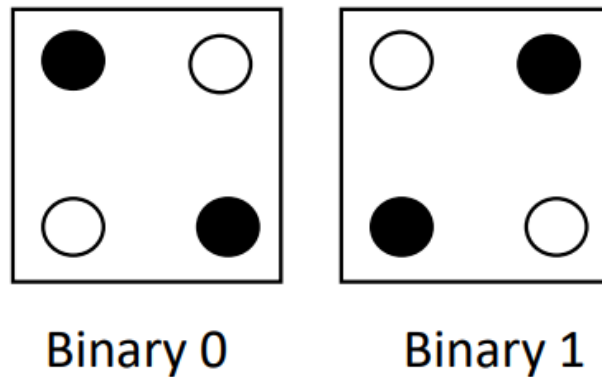


Fig.1: Structure of QCA

The QCA are an appealing rising innovation. The 3-input, 1-output majority gate and the NOT gate are the basic gates of QCA technology using control elite advanced circuits. Hence, over the which we build universal gate (NAND and NOR) and most recent couple of years, the plan of productiveness then any logical circuit can be designed using rationale circuits in QCA has gotten a lot of universal gates. The operation of NOT gate is pretty consideration. Exceptional endeavors are well known to all where the output is just coordinated to number-crunching circuits, with the complement of the input and the operation of 3-input intrigue concentrated on the two-fold input and 1-output gate is a special case where the expansion that is the essential activity of any output is the function of majority of inputs. In advanced framework. Obviously, the model otherwise if the two inputs of the 3-input and 1-regularly utilized in customary CMOS plans are output gate are logic 1 the output is logic 1, viewed as a first reference for the new structure conversely if the two inputs of the 3-input and 1-condition. The CFA was an advanced RCA that output gate are logic 0 the output is logic 0 and moderated effects of impending cables. Parallel hence, sometimes it is also referred as 3-input prefix structures have been dissected and updated majority voter gate. On similar lines 5Maj gate is the in QCA including Bent Kung adder, Kogge-Stone promising one for area and speed optimization and adder and Han Carlson adder. For the CLA and RCA, the functioning 5Maj gate is similar to functioning increasingly effective structures have been 3Maj gate. The output of 5Maj gate will be proposed. In this short, an inventive procedure is logical "1" if at least three inputs of 5Maj gate are introduced to execute fast low-zone adders in QCA. logical "1". On same lines the output of 5Maj gate Theoretical definitions displayed for CLA and will be logical "0" if at least three inputs of 5Maj parallel-prefix adders are here mishandled for the gate are logical "0". As a part of area and speed affirmation of a novel 2-piece extension cut. The optimization of QCA circuits there were a lot of last empowers the bring to be multiplied through technological developments had taken place in the two following piece positions with the deferral of last decade and majority of them are listed here. just a single larger part MG. Similarly, the sharp top For better understating the developments were level building prompts traditionalist configurations, reviewed with respect to circuits that are as needs be avoiding unnecessary clock stages as implemented here. Initially we take a glance at result of long interconnections. A adder arranged as a technical developments of QCA gates, Adders, proposed continues running in the RCA style, yet it RAM's, BCD adders, and finally ends with clocking shows a computational concede lower than all schemes.

condition of the-workmanship contenders and accomplishes the most decreased ADP.

2. Literature Survey

The existing QCA method based digit serial and parallel decimal adders having the same design, but different from the point of majority logics. in [1], [2] literatures, 4-bit ripple carry adder (RCA) based

BCD structures has discussed. But, these designs and other combinational circuits can be effectively need to be optimized to reduce area requirement. designed using the presented adder. The carry look-ahead adder (CLA) approach and Carry implementation of one bit Quantum full Adder flow adder (CFA) approach BCD adders are (QFA) and one bit Full subtractor based on their presented in [3], which show good delay truth table's is given in [9-10] and gives estimation performance, however it has high hardware to build n-bit full adder and n-bit subtractor, which complexity. In literature [4] basic binary adder was requires $4n$ and $8n$ quantum gates respectively. designed and based on it the proficient 4-bit BCD. Similarly, implementation of half adder and half adder was discussed, decreasing wide-rangings subtractor using electron spin is presented based on consumption. For full usage of the QCA gates, in [5] quantum information processing by nuclear and [6] correction logic implemented with less magnetic resonance [11].

majority qca gates. Unlike the offered designs, a **3. Proposed Method**

new method to calculate carry computation in the The block diagram of proposed 1-digit parallel BCD multi-bit BCD adder has discussed in this paper. This adder is shown in fig 2. It consists majorly three paper included decimal group-generate and decimal modules 4 bit binary adder1 unit, Correction logic group-propagate method to calculate carries (CL) using CLA unit and 4 bit binary adder2 unit. As initially, and then sums by using the carries in the it is a 1 digit BCD adder, it is having the inputs A, B BCD adder. Thus, This paper have of 4bits applied to Adder1 unit which is shown in decreased delay, area, power and hardware fig 3. Now adder1 performs the addition operation complexity in the multidigit BCD adder. between A and B, generates BS(binary sum) and

In [7] we can find the basics of Quantum Bcout(binary carry out) as outputs. These outputs Cellular Automata, the device architecture and the are applied to correction logic. It will check the design of 3-input majority gate has laid foundation adder1 output is within the BCD boundaries i.e., 0 to the QCA technology and it can also be viewed to 9, If the adder1 output exceeds the value 9, that it is possible to build quantum devices which Correction operation will perform and results the can implement logical functions as similar to correction value as 6. If the adder1 output does conventional gates. The implementation of both not exceeds the value 9, no need half adder and full adder using QCA AND-NAND have perform Correction operation and results the (ANA) and OR-NOR (O-NO) gates was presented in correction value as 0. The final BCD carry out [7]. The adder circuit design is easy to realize (dCout) is generated across the Correction logic practically with minimum no. of gates using QCA (CL) using CLA unit. Now, the 4 bit binary adder2 is technologies especially with A-NA and O-NO gates. performing the addition operation between the Further other combinational operations like binary adder1 outputs to the Correction logic using multiplexing, subtraction, multiplication, division CLA output.

The final resultant sum (dS) is the BCD value of A, B and cin addition process.

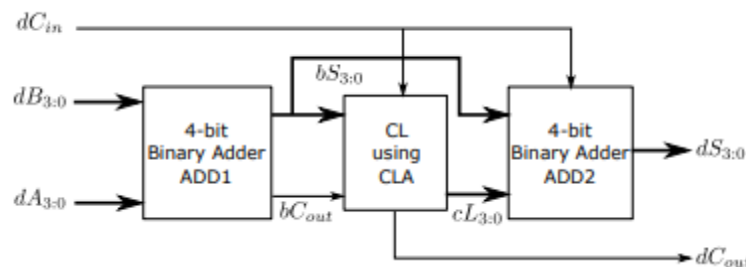


Fig 2. Proposed 4 bit parallel BCD Adder

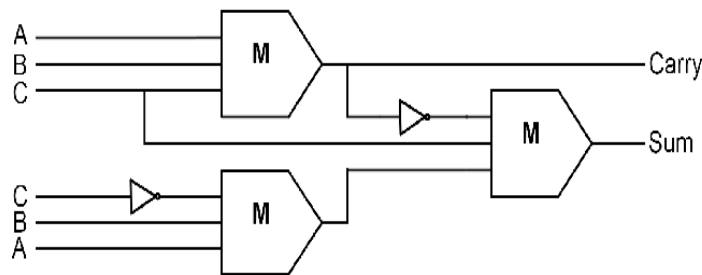


Fig 3. Proposed 1-bit Full adder for Add1

The Figure 3 represents the 1 bit full adder operation, which is implemented by using majority gates and the main use of full adder is we can use it for N-bit addition operations. By using RCA structure, by passing the carry output of first full adder to the next full adder carry input, it is possible to implement N-bit addition. It is also possible to implement By using CLA methodology, CSA methodology or PPA methodology. By using this procedure, the 4 bit binary adder1 unit in the Figure 1 can be developed.

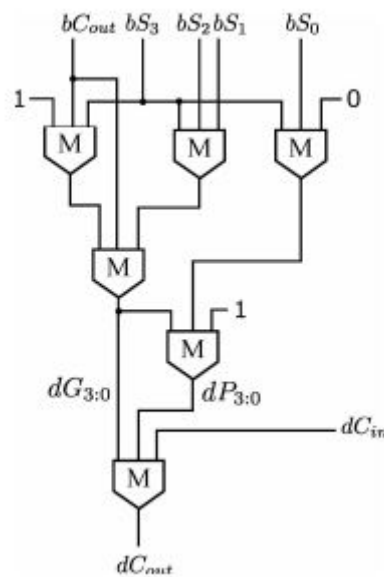


Fig 4. Carry out generation using CL using CLA

The Figure 4 represents the 1 bit Carry out generation process, which is implemented by using majority gates from 4 bits of input. The binary sum, carry out outputs from adder1 unit is applied as inputs here. The majority combinations are used to implement decimal group (dG) and decimal propagate (dP) signals. The dG is signal is generated, if the input bS is greater than or equal to 10. The dP is signal is generated, if the input bS is greater than or equal to 9. Finally by using majority operation between dG, dP and Cin will generate the final resultant carry out. So the final correction value will be generated as CL [3:0] = {0, dcout, dcout, o}.

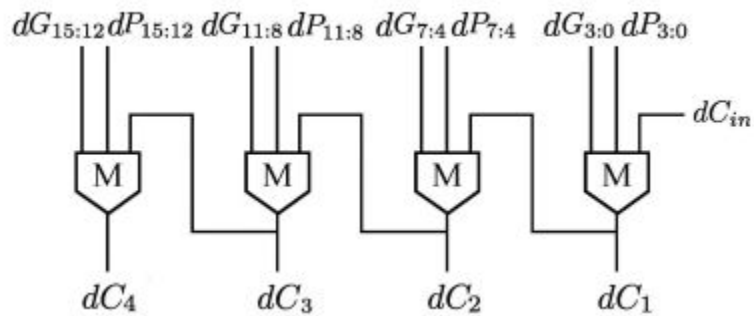


Fig 5. Multiple Carry out generations using CL using CLA

The Figure 5 represents the multiple carry out generation process for 4-digit (16 bit) BCD addition process. Finally by using majority operation between dG, dP and Cin (by passing the carry output of first CL using CLA unit to the next CL using CLA unit carry input) will generate the final resultant carry outs dC₁, dC₂, dC₃ and dC₄.

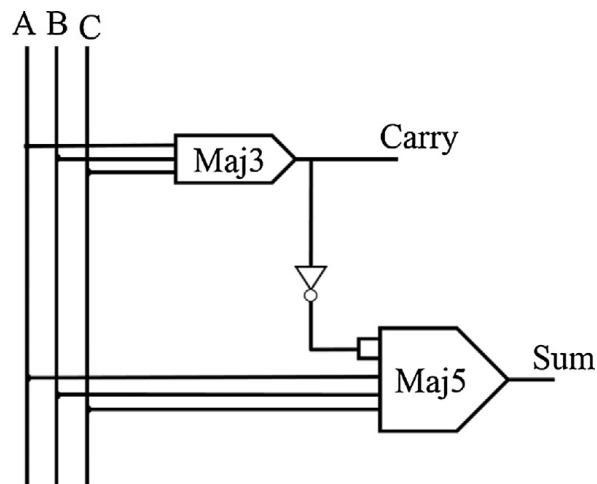


Figure5: Proposed 1-bit Full adder for Add2

Figure6 represents the 1 bit full adder operation, which is implemented by using majority gates of 3 input and 5 input. It is possible to use same full adders for both Adder1 unit and Adder2 unit. But in order to reduce the path delays, area and power consumption, the optimized full adder with two majority gates is preferable as shown in above figure. The main use of full adder is we can use it for N-bit addition operations. By using this procedure, the 4 bit binary adder2 unit in the Figure1 can be developed.

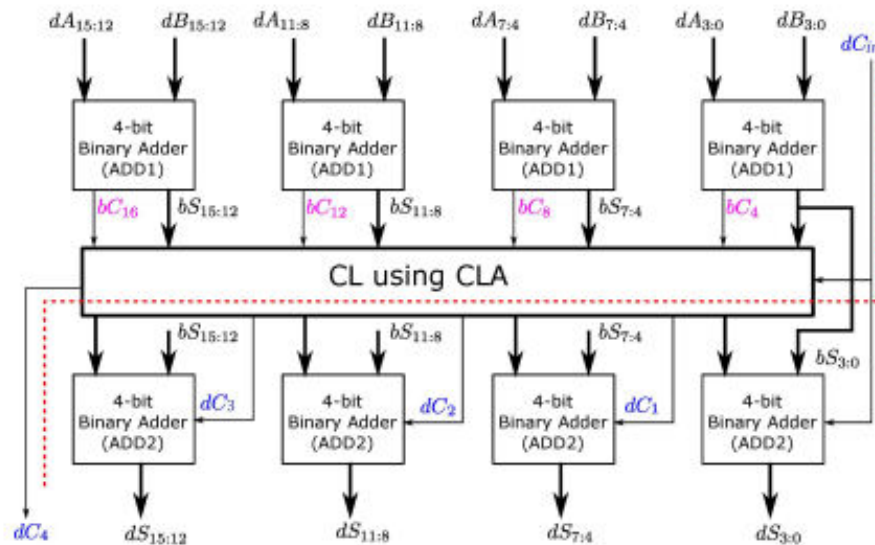


Fig 7. Proposed 4 digit (16 bit) parallel BCD Adder

The Figure 7 represents the 16 bit BCD Adder. All the proposed designs have been programmed and designed using Xilinx ISE software this software in parallel manner. All the adder1 units perform their operation and provides the two categories of outputs named carries (bc16, bc12, bc8 and bc4) and sums (bS[3:0], bS[7:4], bS[11:8] and bS[15:12]) respectively to inputs, output byte level combinations. Now, through simulation analysis of accuracy of the using CLA performs the correction operation addition, multiplication process estimated easily by shown in Figure 6 and generates the correction applying the different combination inputs and by values and corresponding carries (dC1, dC2 and dC3) monitoring various outputs. Through the synthesis the dC4 is the final carry out of BCD operation. All the results the utilization of area with respect to the adder2 units perform their operation as mentioned programmable logic blocks (PLBs), look up tables in Fig 4 in parallel manner. Thus, the resultant sums (LUT) will be achieved. And also time summary with (dS[3:0], dS[7:4], dS[11:8] and dS[15:12]) are the respect to various path delays will be obtained and final BCD sum values. power summary generated using the static and dynamic power consumed.

4. SIMULATION RESULTS

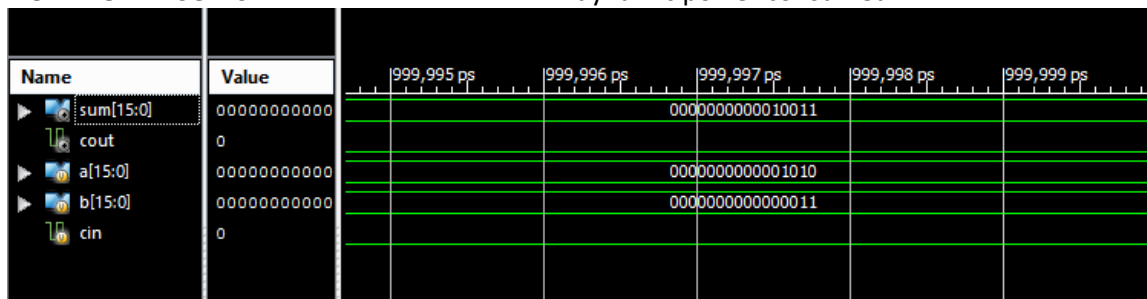


Fig 8: simulation output

The above result represents the simulation waveform by using the Xilinx ISE software. Where N is the length of the adder i.e., 16-bit. Finally, corresponding inputs A, B also 16-bit of values 10 and 3, and cin is 0. Finally, the sum is 32'b 0000 0000 0000 0000 0000 0000 0001 0011, which is in BCD format.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	42	17600	0%
Number of fully used LUT-FF pairs	0	42	0%
Number of bonded IOBs	50	100	50%

Fig 9: Design summary

The above result represents the synthesis implementation by using the Xilinx ISE software. From the above table, it is observed that only 42 look up tables are used out of available 17600. It indicates very less area is used for the proposed design.

Cell: in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF: I->O	2	0.000	0.618	a_2_IBUF (a_2_IBUF)
LUT6: I0->O	4	0.043	0.630	A1/f3/M1/m1 (A1/c2)
LUT6: I0->O	5	0.043	0.626	C1/M6/m (c1<1>)
LUT5: I0->O	2	0.043	0.410	A6/f3/m2/out121 (A6/f3/m2/out12)
LUT5: I3->O	8	0.043	0.642	C2/M6/m1 (c1<5>)
LUT5: I0->O	2	0.043	0.410	A7/f3/m2/out121 (A7/f3/m2/out12)
LUT5: I3->O	7	0.043	0.529	C3/M6/m1 (c1<10>)
LUT3: I0->O	1	0.043	0.405	C4/M6/m3_SW0 (N8)
LUT6: I4->O	4	0.043	0.620	C4/M6/m3 (c1<13>)
LUT6: I1->O	1	0.043	0.339	A8/f2/m2/out1 (sum_13_OBUF)
OBUF: I->O		0.000		sum_13_OBUF (sum<13>)
Total		5.618ns (0.387ns logic, 5.231ns route) (6.9% logic, 93.1% route)		

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Fig 10: Time summary

The above result represents the time consumed such as path delays by using the Xilinx ISE software. the consumed path delay is 5.618ns.

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device	Zynq-7000	On-Chip	Power (W)	Used	Available	Utilization (%)	Supply	Summary	Total	Dynamic	Quiescent		
Family	Zynq-7000	Logic	0.000	34	17600	0	Source	Voltage	Current (A)	Current (A)	Current (A)		
Part	xc7z010	Signals	0.000	75	--	--	Vccint	1.000	0.005	0.000	0.005		
Package	clg400	IOs	0.000	50	230	22	Vccaux	1.800	0.006	0.000	0.006		
Temp Grade	Commercial	Leakage	0.065				Vcco18	1.800	0.001	0.000	0.001		
Process	Typical	Total	0.065				Vccbram	1.000	0.000	0.000	0.000		
Speed Grade	-2						Vccpint	1.000	0.020	0.000	0.020		
							Vccpaux	1.800	0.013	0.000	0.013		
							Vcco_ddr	1.500	0.002	0.000	0.002		
Environment		Thermal Properties	Effective TJA	Max Ambient	Junction Temp		Supply	Power (W)	Total	Dynamic	Quiescent		
Ambient Temp (C)	25.0		(C/W)	(C)	(C)				0.065	0.000	0.065		
Use custom TJA?	No												
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Profile												
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	8 to 11												
Custom TJB (C/W)	NA												

Fig 11: Power summary

The above result represents the power consumed by using the Xilinx ISE software. the consumed power is 0.065w.

Table 1: comparison of 4-bit BCD adder methods

parameter	Conv. BCD ADDER[4]	CMOS BCD ADDER[11]	BCD ADDER[13]	PROPOSED BCD
Time delay(ns)	20.118	13.35	10.34	5.618
Power utilized(uw)	1.293	2.356	1.46	0.065
Look up tables	271	562	72	42
Flip Flops	237	395	103	59



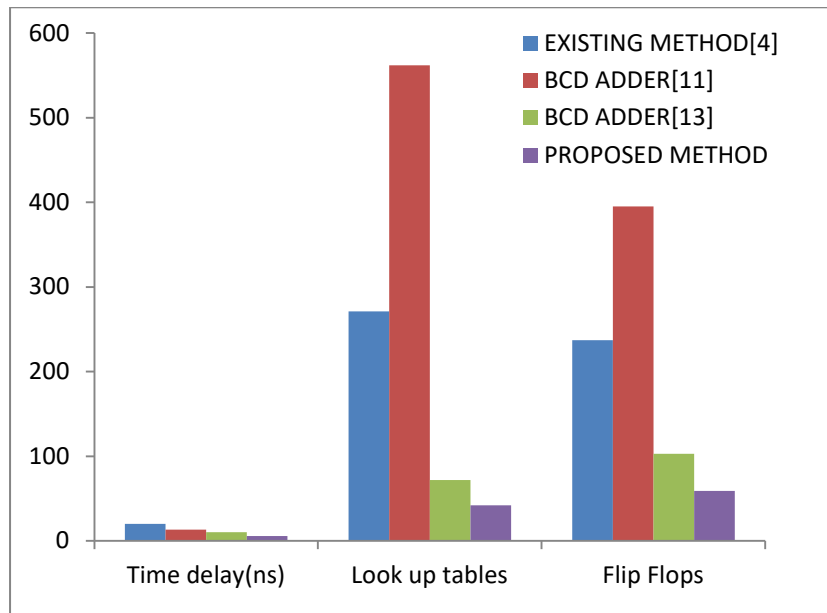


Fig 12: comparison of various methods

Table 2: Performance measurement of BCR adder for various lengths

Adder length	bit	Parameter/ method	Slice registers	LUTs	LUT-FF	Delay (ns)	Power (uW)
8-bit		Conv. BCD ADDER[8]	151	282	22	22	65
		CMOS BCD ADDER[11]	196	365	18	20	104
		BCD ADDER[13]	254	471	28	38	90
		PROPOSED BCD	55	99	15	11	43
16-bit		Conv. BCD ADDER[8]	243	632	38	35	78
		CMOS BCD ADDER[11]	342	733	43	30	178
		BCD ADDER[13]	262	1011	47	53	115
		PROPOSED BCD	142	252	18	17	54
32-bit		Conv. BCD ADDER[8]	853	1264	69	92	113
		CMOS BCD ADDER[11]	1075	1891	63	133	205
		BCD ADDER[13]	1017	2592	63	180	221
		PROPOSED BCD	443	790	36	36	71

From table 1, table 2 and figure 12, it is observed that the proposed BCD adder is area, power and delay efficient compared to the literatures existing method [4], BCD adder [11] and BCD adder [13].

CONCLUSION

Using this QCA technology and Majority gate compared to existing methods.

methodology, new 32 bit Binary coded Decimal

(BCD) adder has developed and discussed its [1] K. Fardad, M. Askari, and M. Taghizadeh, "BCD functionality. The method is simulated and computing structures in quantum-dot cellular synthesized using Xilinx ISE software, simulation automata," in Proc. International Conference on and synthesis (implementation) results have been Computer and Communication Engineering, 2008, verified. The results shown that the proposed method has better performance properties like



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