# A STUDY OF APPROXIMATE MULTIPLIER DESIGN USING ROUNDING METHODS TO SAVE POWER AND ENERGY

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**Abstract:**

Approximate computing is one of finest suited efficient data processing for error resilient applications, such as signal and image processing, computer vision, machine learning, data mining etc. Approximate computing reduces accuracy which is acceptable as a cost of increasing the circuit characteristics depends on the application. Desirable accuracy is the threshold point for controlling the trade off, between accuracy and circuit characteristics under the control of the circuit designer. In this work, the rounding technique is introduced as an efficient method for controlling this trade off. In this regard multiplier circuits as a critical building block for computing in most of the processors have been considered for the evaluation of the rounding technique efficiency. The impact of the rounding method is investigated by comparison of circuit characteristics for multipliers.

***Keywords:*** Multiplicand, Multiplier, Energy efficient, Rounding Technique

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## 1.INTRODUCTION

Energy minimization is one of the main design requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets. It is highly desired to achieve this minimization with minimal performance (speed) penalty. Digital signal processing (DSP) blocks are key components of these portable devices for realizing various multimedia applications. The computational core of these blocks is the arithmetic logic unit where multiplications have the greatest share among all arithmetic operations performed in these DSP systems. Therefore, improving the speed and power/energy-efficiency characteristics of multipliers plays a key role in improving the efficiency of processors. Many of the DSP cores implement image and video processing algorithms where final outputs are either images or videos prepared for human consumption's. This fact enables us to use approximations for improving the speed/energy efficiency. This originates from the limited perceptual abilities of human beings in observing an image or a video. In addition to the image and video processing applications, there are other areas where the exactness of the arithmetic operations is not critical to the functionality of the system. Being able to use the approximate computing provides the designer with the ability of making tradeoffs between the accuracy and the speed as well as power/energy consumption.

Applying the approximation to the arithmetic units can be performed at different design abstraction levels including circuit, logic, and architecture levels, as well as algorithm and software layers. The approximation may be performed using different techniques such as allowing some timing violations (e.g., voltage over scaling or over clocking) and function approximation methods (e.g., modifying the Boolean function of a circuit) or a combination of them. In the category of function

approximation methods, a number of approxima
arithmetic building blocks, such as adders and multipl
at different design levels have been suggested. We f
on proposing a high-speed low power/energy
approximate multiplier appropriate for error resilient
applications. The proposed approximate multiplier, w
is also area efficient, is constructed by modifying
conventional multiplication approach at the algori
level assuming rounded input values.

## 2.LITERATURE SURVEY

**M. Alioto, "Ultra-low power VLSI circuit de
demystified and explained: A tutorial," IEEE Tr
Circuit:**

Wireless sensor networks (WSNs) are today wi
employed in real world applications. However, t
lifetime is still challenging and the most critical limita
for the success of this technology. In fact, wireless sen
nodes, which are the backbone of the network,
typically powered by limited energy storage devices (e.
small batteries or supercaps) and their short lifetime is a
critical issue. Wake-up radio receivers are very effective
minimizing idle listening. This fact has resulted in a
significant number of wake-up radio rece
architectures proposed in last decade. In this work
present an advanced design and implementation of
advanced wake-up radio that is capable of
processing the received data (i.e. for addressing)
retransmitting data or wake up messages to
neighbours when necessary. With these features it can
possible to further enhance the energy efficiency of
communication and allowing ultra-low power multi-
communication. Experimental results demonstrate
functionality as well as the power and range of
proposed design which is ready for future energy effic
and pure-asynchronous MAC protocols.

**V. Gupta, D. Mohapatra, A. Raghunathan, and K. I
"Low-powerdigital signal processing using approxim
adders," IEEE Trans. Comput.-Aided Design Int
Circuits:*IEEE Trans.***

Low power is an imperative requirement for porta
multimedia devices employing various signal proces
algorithms and architectures. In most multim
applications, human beings can gather useful informa
from slightly erroneous outputs. Therefore, we do
need to produce exactly correct numerical outputs.
Previous research in this context exploits error resiliency
primarily through voltage over scaling, utilizing
algorithmic and architectural techniques to mitigate the
resulting errors. In this paper, we propose logic
complexity reduction at the transistor level as an
alternative approach to take advantage of the relaxation
of numerical accuracy. We design architectures for video
and image compression algorithms using the proposed
approximate arithmetic units and evaluate them to
demonstrate the efficacy of our approach. We also derive
simple mathematical models for error and power
consumption of these approximate adders. Furthermore,
we demonstrate the utility of these approximate adders
in two digital signal processing architectures (discrete
cosine transform and finite impulse response filter) with
specific quality constraints. Simulation results indicate up
to 69% power savings using the proposed approximate
adders, when compared to existing implementations
using accurate adders.

**H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas,
"Bio-inspiredimprecise computational blocks for efficient
VLSI implementation of soft-computing applications,"
IEEE Trans. Circuit*:***

The conventional digital hardware computational blocks
with different structures are designed to compute the
precise results of the assigned calculations. The main
contribution of our proposed Bio-inspired Imprecise
Computational blocks (BICs) is that they are designed to
provide an applicable estimation of the result instead of
its precise value at a lower cost. These novel structures
are more efficient in terms of area, speed, and power
consumption with respect to their precise rivals.
Complete descriptions of sample BIC adder and multiplier
structures as well as their error behaviors and synthesis
results are introduced in this paper. It is then shown that
these BIC structures can be exploited to efficiently
implement a three-layer face recognition neural network
and the hardware defuzzification block of a fuzzy
processor.

**R. Venkatesan, A.Agarwal, K. Roy, and A.Raghunathan,
"MACACO:Modeling and analysis of circuits for
approximate computing," in Proc. Int. Conf. Comput.
Aided Design:**

Approximate computing, which refers to a class of
techniques that relax the requirement of exact
equivalence between the specification and

implementation of a computing system, has attracted significant interest in recent years. We propose a systematic methodology, called MACACO, for the Modeling and Analysis of Circuits for Approximate Computing. The proposed methodology can be utilized to analyze how an approximate circuit behaves with reference to a conventional correct implementation, by computing metrics such as worst-case error, average-case error, error probability, and error distribution. The first step in MACACO is the construction of an equivalent untimed circuit that represents the behavior of the approximate circuit at a given voltage and clock period. Next, we construct a virtual error circuit that represents the error in the approximate circuit's output for any given input or input sequence. Finally, we apply conventional Boolean analysis techniques (SAT solvers, BDDs) and statistical techniques (Monte-Carlo simulation) in order to compute the various metrics of interest. We have applied the proposed methodology to analyze a range of approximate designs for datapath building blocks. Our results show that MACACO can help a designer to systematically evaluate the impact of approximate circuits, and to choose between different approximate implementations, thereby facilitating the adoption of such circuits for approximate computing.

**F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, "New approximate-multiplier for low power digital signal processing"**

In this paper a low power multiplier is proposed. The proposed multiplier utilizes Broken-Array Multiplier approximation method on the conventional modified Booth multiplier. This method reduces the total power consumption of multiplier up to 58% at the cost of a small decrease in output accuracy. The proposed multiplier is compared with other approximate multipliers in terms of power consumption and accuracy. Furthermore, to have a better evaluation of theproposed multiplier efficiency, it has been used in designing a Gaussian low pass FIR filter and the power consumption and accuracy are compared with that of a filter with conventional booth multipliers. The simulation results show a 17.1% power reduction at the cost of only 0.4 dB decrease in the output SNR.

## 3.EXISTING SYSTEM

Luigi WALLACE, the computer scientist has invented the WALLACE hardware multiplier during 1965. WALLACE multiplier is extracted form of parallel multiplier [5]. It is slightly faster and requires fewer gates. Different types of schemes are used in parallel multiplier. The WALLACE scheme is one of the parallel multiplier schemes that essentially minimize the number of adder stages required to perform the summation of partial products.

This is achieved by using full and half adders to reduce the number of rows in the matrix number of bits at each summation stage. Even though the WALLACE multiplication has regular and less complex structure, the process is slower in manner due to serial multiplication process. Further, WALLACE multiplier is less expensive compared to that of Wallace tree multiplier. Hence, in this paper, WALLACE multiplier is designed and analysed by considering different methods using full adders involving different logic styles.

**Wallace Tree Multiplier Using Ripple Carry Adder**

Ripple Carry Adder is the method used to add more number of additions to be performed with the carry in and carry outs that is to be chained. Thus multiple adders are used in ripple carry adder. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. The proposed architecture of WALLACE multiplier algorithm using RCA is shown in Figs.9 to 11 Take any 3 values with the same weights and gives them as input into a full adder. The result will be an output wire of the same weight. Partial product obtained after multiplication is taken at the first stage. The data's are taken with 3 wires and added using adders and the carry of each stage is added with next two data‟s in the same stage. Partial products reduced to two layers of full adders with same procedure. At the final stage, same method of ripple carry adder method is performed and thus product terms p1 to p8 is obtained.

## 4.PROPOSED SYSTEM

The main idea behind the proposed approximate multiplier is to make use of rounded input for multiplication. Proposed algorithm applies a rounding technique before passing the data to the partial product generation. Fig. 1 shows the design chart for realization of the proposed method for the approximate multiplier design. Among the two inputs (Multiplicand and Multiplier), the Multiplier is rounded first by passing through rounding block. Before the multiplication

operation starts, the sign bit of both inputs is stored, and the output sign of the multiplication result based on the inputs signs are determined. At the last stage, the product sign is applied to the result. In an event of multiplying negative numbers, the respective input blocks are converted into their 2's complement.

In conventional multipliers, with N-bit input, N × N partial products (partial products) are generated. But in the rounding technique, the partial products generated are the combination of active and inactive partial products. The active partial products are, that have "1" as the coefficient on the Multiplier. After rounding, it causes a complete row of Multiplicand as the result. Therefore, inactive partial products are the lines with whole 0's. Therefore, has no necessity to cover them in the reduction process.

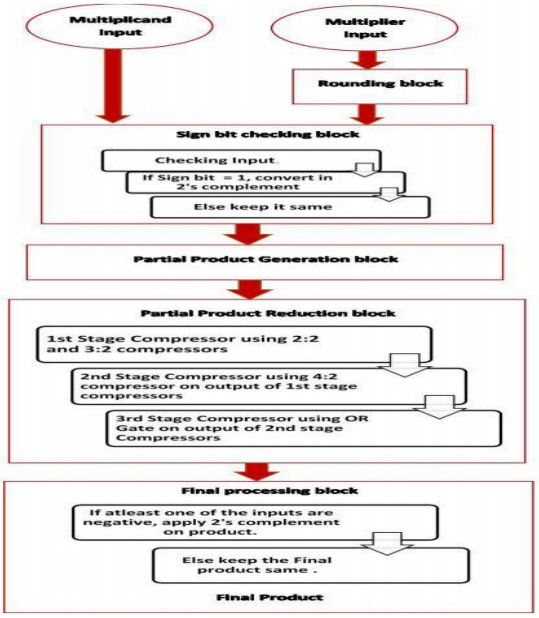


Fig. 1: 16-bit Block diagram of the algorithm

Rounding input data requires major responsibility in maintaining the accuracy. With a basic intuition, it can be stated that, rounding lower bits results in less error compared to rounding higher bits. Thus, the proposed algorithm has assigned rounding weights with respect to the bit position value. There is a small error gap between accurate bit position and rounded bit position. For every accurate bit, there is a corresponding rounded bit value assigned. Error gap reduces as the bit position value increases. Fig. 2 gives an example where 'A' and 'B' are inputs and input 'B' is rounded to get 'Br'. "Rounding Technique" basically checks for a '1' in the 'X' bit position and assigns '1' to the respective 'Y' bit position with or without a small error.

| Accurate Bit Position | Approximate Bit Position |
|---|---|
| bit0 | bit1 |
| bit1 | bit1 |
| bit2 | bit1 |
| bit3 | bit4 |
| bit4 | bit4 |
| bit5 | bit4 |
| bit6 | bit7 |
| bit7 | bit7 |
| bit8 | bit7 |
| bit9 | bit10 |
| bit10 | bit10 |
| bit11 | bit10 |
| bit12 | bit13 |
| bit13 | bit13 |
| bit14 | bit15 |
| bit15 | bit15 |

= 0001 0011 1000 1000
= 0000 0011 1111 1111
= 0000 0100 1001 0010

15 13 10 7 4 1
Leads to active partial product rows

Fig. 2: An example after rounding 'B' (16-bit)

Partial products reduction is a stage where partial products are compressed using different kind of compressors. Proposed algorithm gives a flexibility on reducing number of partial products rows. For an instance 16-bit design shown in Fig. 3 reduces partial products to 6 rows which is identified as active partial products. Like all traditional way, N-bit inputs are multiplied to generate N × N Partial products. In terms of computation complexity, as the number of bitsincreases, the length of Partial products increases with $O(N^2)$. Proposed algorithm provides computation complexity ≤ O(N×6) for 16-bit and ≤ O(N×13) for 32bit. For better understanding, along with design, an example is explained with input values A, B and Br (from fig. 6(right)). Multiplier input 'B' is first rounded to 'Br'. Inputs are then multiplied to get N×N partial products. Due to rounding of multiplier input, N×N partial products is a combination of active and inactive partial products. Multiplier with '1' as coefficient, after rounding, causes a complete row of Multiplicand as a result as illustrated in fig. 3. Therefore, inactive partial products are the whole zero values line which had "0" as the coefficient

on the Multiplier. Thus, there is no need to cover them in the reduction process. In fact, inactive partial products could only increase hardware. This has led us to first eliminate, all inactive partial products before packing. This approach plays important role in reducing power, area and time usage and in turn increasing its efficiency. The active partial products are compressed and packed using three stages of compression. In the 1st stage, partial products are compressed using full adders and half adders. An output of 1st stage compression is further compressed using a 4:2 compressor when inputs are 16bit whereas for 32bit, 9:2 compressor. Fig. 3 (right) illustrates corresponding operations on an example. An output of the 2nd stage compressor is finally packed using OR gate to get a final product. Conventionally full adders are used instead of OR. The very idea of using OR gate instead of full adder is to reduce area and energy usage noticeably.

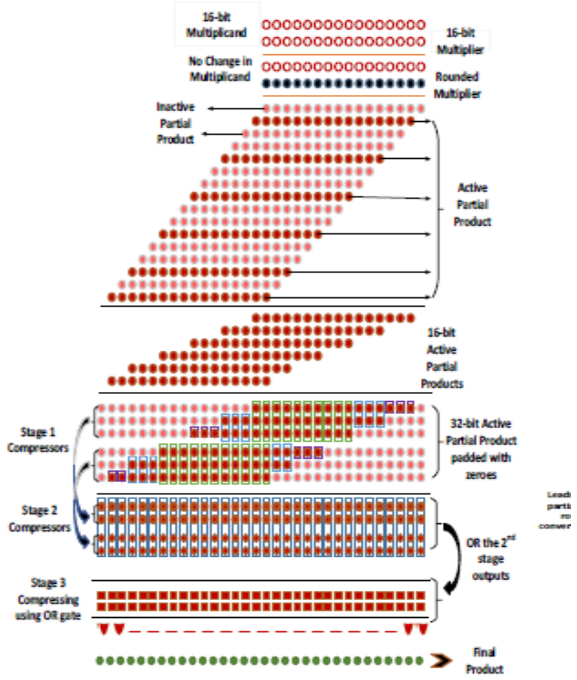


Fig. 3: Multiplier Design (left) with an example (right) (16-bit).

## 5.SIMULATION RESULT OF MULTIPLIER:

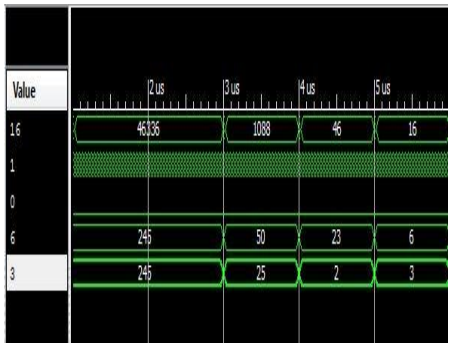


Fig 4 Simulation Result of Multiplier

Here we can give the inputs as A=6, B=3, clk as 1 and rst as 0, then the final output is 16.

## 6. CONCLUSION

Proposed algorithm proves to be best in terms of power-area delay and PDP efficiency when compared to other algorithms for both signed and unsigned data (16-bit and 32-bit). This is the primary investigation of rounding technique on approximate multiplier by having one method of rounding pattern which are fixed active partial product rows. With this rounding pattern, we see potential areas of less accuracy and areas with better accuracy corresponding to probability of rounding value. Based on accuracy required, rounding patterns are changed with a little extra expense of hardware. Rounding pattern can be modified to have fixed or dynamic partial product rows and yet have fewer active partial product rows for compression. The proposed algorithm can be used in the wide range of applications in image processing, machine learning and signal processing. Thus, different weights based on the bit position of '1' plays an important role to keep accuracy relatively near to the conventional method. With flexible reduction of partial products, proposed algorithm produces great hardware characteristics, when compared to DRUM.

## 7.FUTURE SCOPE

This multiplier plays a very important role in our day to day life. In future the multipliers are going to play a major role. The speed of the multipliers are increased by using carry save adders, carry look ahead adder, and so on. Rounding patterns will be optimized based on required accuracy and different compression techniques. The area and delay can be reduced in future by using advanced technology.

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