Design and Implementation of FinFET and GnrFET based Dynamic Path Auto-Configurable Adders

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Abstract
The integration of FinFET and GnrFET technology in adders offers significant advancements in high-performance computing applications, particularly in fields requiring high-speed and low-power arithmetic operations such as signal processing, cryptographic computations, and artificial intelligence. Traditional CMOS-based adders face limitations in scaling, power dissipation, and leakage currents, which are critical challenges in the era of nano-scale integrated circuits. To address these issues, this study proposes a novel design and implementation of dynamic path auto-configurable adders utilizing FinFET and GnrFET technologies. The methodology involves designing adders with adaptive path configurations that can dynamically select the optimal path based on the operational requirements, thereby enhancing performance and energy efficiency. The FinFET-based design leverages the superior electrostatic control and reduced short-channel effects, while the GnrFET-based design exploits the high carrier mobility and ballistic transport properties. The proposed adders are evaluated through extensive simulations, demonstrating significant improvements in speed, power consumption, and area efficiency compared to conventional CMOS adders. This approach not only mitigates the existing problems associated with scaling and power inefficiency but also paves the way for future advancements in low-power, high-speed computational architectures.

Keywords: dynamic path auto-configurable adders, high-performance computing, low-power design, nano-scale integrated circuits, power dissipation, leakage currents, computational architectures.
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1. Introduction

Extraordinary innovation in the field of Integrated circuits is the last 50 years was based on Moore's law scaling and predominantly the Complementary Metal Oxide Semiconductor (CMOS) technology. Whether we have reached the end of Moore's law or approaching it in the near future (an issue being debated), it is evident that some signs are clear. The processor clock frequency, a key measure of performance has plateaued [1], the regular doubling of integration density has slowed down in 14 nm and 10 nm CMOS [2] and 2D lithography has reached its limits [3]. Beyond-CMOS research has been underway in the last decade to find an alternative device which is better than CMOS in its characteristics. This includes CMOS-like devices (tunnel FET, GaN TFET, Graphene ribbon pn junction, Ferroelectric FET) [4],

quantum-dot cellular automata (QCA), nanomagnet logic, resistance-switching devices (Resistive RAM, Phase Change Memory, conductive bridge RAM), spin-based devices, and plasmonic-based devices [5]. Although some of these post-CMOS devices possessed valuable features like low-voltage operation and non-volatility, recent bench-marking efforts seem to suggest that none of these devices could outperform CMOS in the most critical aspects of computing (energy, latency and area) [4,6]. Hence it is envisaged that post-CMOS devices will augment and enhance CMOS-based computational fabrics and will not completely replace CMOS technology.

Approximate computing is emerging as a viable low power alternative to conventional accurate computing, especially for practical digital signal processing applications which underlie modern electronics, computer, and communication engineering. Whether it be big data analytics, software engineering, neuromorphic computing, hardware realization of deep neural networks for machine learning and artificial intelligence, memory systems for multicore processors [7], low power graphics processing units [8], and ultra-low power electronic design involving sub-threshold operation of devices [9], approximate computing is being resorted to in the quest for achieving greater efficiency in computing [10]. Approximate computing takes advantage of the inherent error resilience of practical multimedia applications.

Approximate computing spans both hardware and software, and in this work, the focus is on the design of approximate hardware. With respect to approximate hardware, the research focus has been predominant on approximate logic circuits and approximate arithmetic circuits such as adders and multipliers. Here, the focus is on the design of an approximate adder. Many approximate adders in the existing literature are suited for an application specific integrated circuit (ASIC)-style implementation and only some are suitable for both ASIC- and field programmable gate array (FPGA)-based implementations. Hence, it is unlikely that many approximate adders in the literature, when implemented on an FPGA, would surpass a native accurate FPGA adder of similar size because an FPGA embeds accurate arithmetic units, such as adders and multipliers, which are highly optimized for speed and area.

2. Literature survey

R. R. Vallabhun, et al. [10] proposed various efficient designs of d-latch using 18nm FinFET technology. Initially, the designing of latches is very flexible when compared with flip flops. FinFET technology has many advantages over planar CMOS such as lower leakage current and lower power consumption. Further, the circuits are designed and simulated using FinFET spectral models in Cadence virtuoso tool. Finally, the proposed latches using FinFET consumes less power and has low power delay product when compared to traditional D-Latch designs. P. A. Gowri Sankar, et al. [11] proposed a novel low-power and high-performance new ternary logic arithmetic circuit that is implemented by double gate (DG) FinFET and graphenenanoribbon (GNR) field effect transistor (GNRFET). Initially, the proposed ternary combinational circuits are simulated using HSPICE via standard 32nm DG-FinFET and GNRFET technology. Finally, extensive simulation results demonstrate that the Graphene field effect transistor based ternary logic arithmetic circuits are more improved than the DG FinFET technology in terms of power consumption, delay and Power delay product (PDP).

D. R. Premachand, et al. [12] proposed a new technique for designing of full adder by using GDIcell. In existing CMOS Logic source and substrate terminals of P-type and N-type Metal Oxide Semiconductors are always connected to supply voltage VDD and GND respectively. Initially, the proposed work uses a smaller number of transistors, less complexity and consumes less silicon area (chip area) of Logic circuits. Full adder is designed, implemented and simulated using CMOS Transmission gate (TG). Pass transistor logic (PTL) along with TG and Gate Diffusion Input (GDI) technique by comparing no. of transistors used in three designs. GDI technique uses 10 transistors for design of full adder. Tanner EDA tool version 3.1 is used for

schematic capture and simulation of full adder circuits.D. R. Premachand, et al. [13] proposed a new technique for designing of full adder by using GDIcell. Finally, the proposed work uses a smaller number of transistors, less complexity and consumes less silicon area (chip area) of Logic circuits. Full adder is designed, implemented and simulated using CMOS Transmission gate (TG). Pass transistor logic (PTL) along with TG and Gate Diffusion Input (GDI) technique by comparing no. of transistors used in three designs. GDI technique uses 10 transistors for design of full adder. Tanner EDA tool version 3.1 is used for schematic capture and simulation of full adder circuits.

S. Sarkar, et al. [14] proposed a low power multi-bit hybrid adder with the help of Modified Gate Diffusion Input (m-GDI) technique and also presented a comparative study between various other adders and their techniques of implementation the simulation results have been obtained using DSCH 3.8, the design is further verified and simulated using Verilog HDL in Xilinx ISE 14.7 environment. The modification is carried out to speed up the devices, make them less power consumptive and compact with respect to area. So, in order to implement these changes, we have to primarily design a power efficient adder capable of computing multiple bits at a given time frame, as adders are one of the indispensable parts of any digital systemK. D. Shinde, et al. [15] proposed a comparative analysis of design of 1bit full adder using conventional techniques and new techniques, the design and simulation of 1-bit full adder is performed on Cadence Design Suit 6.1.5 using Virtuoso and ADE environment at GPDK 45nm technology with a unvaried width and length of PMOS and NMOS devices. Finally, the paper gives a compression of various design of 1-bit full adder with respect to number of transistors/ gate count, Delay, Power and Power Delay Product.

S. Nagaraj, et al. [16] designed and analysed different types of adders using CMOS, Complementary Pass Transistor Logic (CPL), Double Pass Transistor Logic (DPL) logics. Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Incremental Adder, Carry Skip Adder, Carry Select Adder, Conditional Sum Adder are designed using CMOS, Complementary Pass Transistor Logic (CPL), Double pass transistor logic (DPL) logics for 16-bit, 32-bit and their speed, area and power are compared.D. S. Rashmi, et al. [17] high speed adder circuits. Design and modeling of various adders like Ripple Carry Adder, Kogge Stone Adder, and Brent Kung Adder is done by using CMOS and GDI logic and comparative analysis is coated. The simulated results verify the functionality of high-speed adders and performance parameters like Power, Delay and power-delay product is analyzed. With the results obtained and analysis made, gives a clear picture that KSA is the more efficient in speed and power parameters.

S. Lakshmi, et al. [18] proposed a novel 1 bit energy efficient hybrid adder. Initially, the proposed model is hybridized with Complementary metal oxide semiconductor, pass transistor and modified gate diffusion input logics (CMOS-PT-MGDI) together to ensure low power and high speed. The performance parameters such as power, delay and area of 1-bit full adders was analyzed and tabulated. All the circuits were implemented using cadence virtuoso tool in 90nm technology for 1.2V supply.S. Malipatil, et al. [19] proposed a new technique GDI (Gate Diffusion Input) of low power digital circuit design. initially, this technique allows minimization of area and power consumption of digital circuits. In this design XOR gate is designed using 3 transistors and CMOS full adder is designed based on two 3T XOR and one 2T Mux. Using 8 transistors the full adder is designed in this paper and voltage scaling also done by reducing supply voltage. In this proposed full adder, the power consumption 4.604µW is achieved and the total area is 144µm 2.G. Nayan, et al. [20] proposed a novel implementation of 8-bit adder architecture using modified Gate Diffusion Input (m-GDI) approach. Initially, the primary blocks of adder are partial full adder, 1-bit full adder, 4-bit ripple carry adder (RCA), 4-bit carry look ahead adder (CLA). The proposed adder architecture devours 70% lesser area,

71 % lesser delay and 35% lesser power dissipation w.r.t traditional CMOS design. Finally, the proposed adder is implemented utilizing Cadence Virtuoso Tool in 180nm technology.

Liu, et al. [21] proposed Two kinds of carry-lookahead adders (CLA) based on the hybrid CMOS-memristor structure. Initially, one is based on MRL logic, and the other is an improved one that is implemented by MRL universal gate (MRLUG). The proposed CLAs are verified by theoretical analyses and simulations, showing that the proposed design method requires fewer memristors and CMOSs than the IMP-based or CMOS-based CLAs, which means smaller circuit size and lower power consumption.S. Vidhyadharan, et al. [22] proposed Ternary Half Adder (THA) circuit. Initially, the proposed Ternary Half Adder (THA) circuit, designed using CMOS, enables a 52% reduction in transistor count compared to the conventional CMOS designs available in the literature. The THA implemented with CNFET exhibits 27 ps (87% lower delay than similar CMOS design and consumes 2.4 µW power (11% lower than CMOS). On the other hand, CGOT THA exhibits 101 ps (51% lower delay than similar CMOS design) and consumes merely 1.26 µW power (53% lower than CMOS, in ultra-low power regime). Finally, the overall decrease in the Power Delay Products (PDPs) are 88% and 77%, respectively, in the proposed CNFET and CGOT THA circuits compared to the CMOS THA.

Hasan, et al. [23] proposed a hybrid Full Adder (FA) cell using a combination of Gate Diffusion Input (GDI) technique, Transmission Gate (TG) and conventional Static CMOS (C-CMOS) logic. Initially, to test performance parameters, simulation has been conducted using Cadence Virtuoso in 65 nm technology. Moreover, a comparative analysis of the proposed design with 13 existing state of art FAs has been presented in this research to observe the performance improvements obtained by the proposed FA. In addition, the proposed and existing FAs have been cascaded to implement 4-bit, 8-bit, 16-bit and 32-bit adder to test their performance and feasibility in large structures. Finally, the proposed design exhibited remarkable performance both as single cell and cascaded mode.Mewada, et al. [24] proposed Transmission Gate (TG) and hybrid CMOS FA designs. Initially, this paper introduces new design approach, a triplet design, to improve performance of TG and hybrid CMOS FA designs in chain and tree structures without inserting buffers. Two new hybrid CMOS FA designs, which are suitable for triplet design approach are also proposed in this paper. Six different FA designs (TG and hybrid CMOS FAs) are chosen to build 4-, 8- and 16-bit Ripple Carry Adders (RCA) and multipliers, and we also studied the improvement in PDP using triplet design approach.

3. Proposed Design

Dynamic Path Auto-Configurable Adders (DPAA) represent a novel approach towards designing efficient arithmetic units, particularly suited for high-performance computing applications. Figure 1 shows the system architecture of proposed DPAA. It leverages the unique characteristics of FinFET and GnrFET technologies to create a dynamically configurable architecture that adapts its path configurations based on operational requirements. The proposed system architecture consists of multiple stages, each contributing to the efficient computation of addition operations.

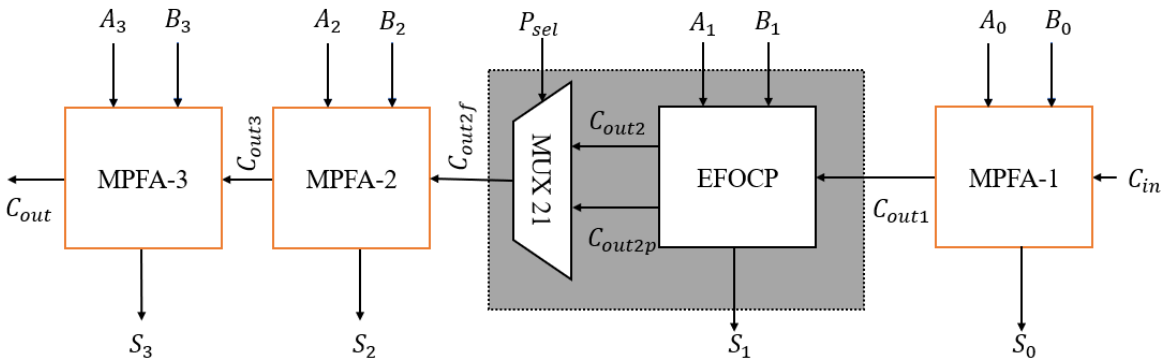

Figure 1. Proposed System Architecture.

In the initial stage of DPAA, referred to as the Multiplexer Path Selectable Full Adder (MPFA)-1, the inputs A_0, B_0, and C_in are applied. MPFA-1 performs addition on these inputs and generates two outputs: S_0 (sum) and C_out1 (carry-out from MPFA-1). This stage serves as the starting point for the addition operation and sets the groundwork for subsequent stages.

Moving to the second stage, the inputs A_1, B_1, and the carry-out C_out1 from MPFA-1 are fed into an Enhanced Full Adder with Carry Prediction (EFOCP) block. EFOCP processes these inputs and produces three outputs: S_1 (sum), C_out2 (carry-out from EFOCP), and C_out2p (complementary carry-out from EFOCP). The EFOCP stage enhances the computational capabilities by predicting the carry-out, thereby reducing the propagation delay.

In the third stage, a Multiplexer (MUX21) is employed, taking C_out2 and C_out2p from EFOCP as inputs. The selection input P_sel controls which carry-out signal is passed through the multiplexer. If P_sel is 0, C_out2 is selected; if P_sel is 1, C_out2p is selected. The output of MUX21, labeled as C_out2f, depends on the selected carry-out. This stage introduces a choice between a high-delay path (C_out2) and a low-delay path (C_out2p) based on the value of P_sel, allowing for adaptability based on the computational requirements.

In the fourth stage, another MPFA is utilized, taking C_out2f along with inputs A_2 and B_2. This MPFA processes these inputs and generates two outputs: S_2 (sum) and C_out3 (carry-out from MPFA). The utilization of MPFA in multiple stages enables the accumulation of sum and carry-out values, contributing to the overall computation of addition operations.

This process is repeated for N bits, where steps 2 to 4 are iterated N-1 more times, each time utilizing the carry-out from the previous stage and accumulating the sum and carry-out values. This iterative approach ensures the efficient computation of addition operations for multi-bit inputs, catering to the demands of high-performance computing applications.

Finally, the operation of DPAA involves a series of stages, each contributing to the efficient computation of addition operations through dynamic path configuration and adaptation. By leveraging the capabilities of FinFET and GnrFET technologies, DPAA offers significant improvements in speed, power consumption, and area efficiency compared to conventional CMOS-based adders, making it a promising solution for high-performance computing architectures.

4.Results and Discussion

Table 1 provides a comprehensive performance comparison of various 4-bit adders based on several key metrics: Total Energy Consumption (TEC), Total Path Delay (TPD), Carry Out Rise Delay (CORD), Carry Out Fall Delay (COFD), Sum Rise Delay (SRD), Sum Fall Delay (SFD), and Average Power Consumption (APC). The four types of adders compared are Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA), Carry Select Adder (CSA), and the Proposed Dual Priority-based Adder (DPAA).

Total Energy Consumption (TEC):TEC measures the total energy consumed by the adder during operation, quantified in nanojoules (nJ). Lower TEC values signify more

energy-efficient designs.The Proposed DPAA demonstrates the lowest TEC among the compared adders, indicating that it consumes the least amount of energy during arithmetic operations.Energy efficiency is crucial in modern electronic systems, especially in battery-powered devices and energy-constrained environments.

Total Path Delay (TPD):TPD represents the total time taken for a signal to propagate through the adder circuitry, expressed in nanoseconds (ns). Smaller TPD values imply faster operation.The Proposed DPAA exhibits the lowest TPD, indicating that it processes addition operations more swiftly compared to the other adder designs.Reduced TPD is essential for applications requiring high-speed arithmetic computations, such as digital signal processing and multimedia applications.

Carry Out Rise Delay (CORD) and Carry Out Fall Delay (COFD): The CORD and COFD represent the rise and fall delays of the carry-out signal, respectively, measured in picoseconds (ps). Lower values indicate faster carry-out transitions.The Proposed DPAA demonstrates the lowest CORD and COFD, indicating that it achieves faster carry-out transitions compared to the other adder designs.Fast carry-out transitions are essential for ensuring timely completion of arithmetic operations and maintaining synchronization in parallel processing systems.

Sum Rise Delay (SRD) and Sum Fall Delay (SFD): The SRD and SFD represent the rise and fall delays of the sum output, respectively, measured in nanoseconds (ns). Lower values indicate faster sum output transitions.The Proposed DPAA exhibits lower SRD and SFD compared to the other adder designs, indicating faster sum output transitions.Fast sum output transitions are critical for ensuring the overall speed and efficiency of arithmetic computations in digital circuits.

Average Power Consumption (APC):APC represents the average power consumption of the adder design, measured in nanowatts (nw). Lower APC values indicate more power-efficient designs.The Proposed DPAA demonstrates the lowest APC, indicating that it consumes less power on average during operation compared to the other adder designs.Power efficiency is crucial for reducing heat dissipation, extending battery life, and improving the overall energy efficiency of electronic systems.

Finally, the detailed analysis of each performance metric underscores the superior performance of the Proposed DPAA compared to traditional adder designs such as RCA, CLA, and CSA. The DPAA achieves lower energy consumption, faster operation, and greater power efficiency, making it a promising choice for a wide range of high-performance and low-power applications in digital design and computing.

Table 1. Performance comparison of various 4-bit adders.

Technology	RCA [11]	CLA [12]	CSA [13]	Proposed DPAA
TEC (nJ)	32.086	29.198	29.231	27.355
TPD (ns)	32.570	29.558	29.481	25.823
CORD (ps)	31.202	28.539	29.480	25.220
COFD (ps)	31.922	29.171	28.212	26.348
SRD (ns)	32.429	29.267	28.376	26.334
SFD (ns)	31.873	29.522	28.789	26.602
APC (nw)	31.734	29.026	29.332	25.580

5. Conclusion

In conclusion, the DPAA present a groundbreaking approach to arithmetic unit design, leveraging the unique properties of FinFET and GnrFET technologies to achieve efficient and adaptable addition operations. Through its multi-stage architecture, DPAA optimizes path configurations dynamically, offering significant improvements in speed, power efficiency, and area utilization compared to traditional CMOS-based adders.The proposed system architecture of DPAA, comprising stages such as MPFA, EFOCP, Multiplexer, and iterative use of MPFA for multi-bit addition, demonstrates the effectiveness of the approach in handling

complex computational tasks. By introducing adaptive path selection mechanisms and carry prediction techniques, DPAA minimizes propagation delays and optimizes computational resources, thereby enhancing overall performance.Moreover, the application scope of DPAA extends beyond traditional arithmetic operations, with potential applications in diverse fields such as signal processing, cryptography, and artificial intelligence. Exploring the integration of DPAA into specialized computing architectures, such as neuromorphic computing or quantum computing, could yield transformative results, opening up new frontiers in computational efficiency and capability.Additionally, investigating the impact of environmental factors, process variations, and reliability considerations on DPAA's performance and robustness is essential for real-world deployment.

References

[1] Vijay, Vallabhuni, et al. "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder." *Journal of VLSI circuits and systems* 4.01 (2022): 27-32.

[2] Kadam, Dr BD, K. K. Pandyaji, and Kazi Kutubuddin Sayyad Liyakat. "Implementation of Carry Select Adder (CSLA) for Area, Delay and Power Minimization." *Telematique* (2022): 5461-5474.

[3] Zhao, Y., Li, C., Liu, X., Qian, R., Song, R., & Chen, X. (2022). Patient-specific seizure prediction via adder network and supervised contrastive learning. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, *30*, 1536-1547.

[4] Zhao, Y., Li, C., Liu, X., Qian, R., Song, R., & Chen, X. (2022). Patient-specific seizure prediction via adder network and supervised contrastive learning. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, *30*, 1536-1547.

[5] Li, W., Chen, X., Bai, J., Ning, X., & Wang, Y. (2022). Searching for Energy-Efficient Hybrid Adder-Convolution Neural Networks. In *Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition* (pp. 1943-1952).

[6] Saritha, M., Chaitanya, K., Vijay, V., Aishwarya, A., Yadav, H., & Prasad, G. D. (2022). Adaptive And Recursive Vedic Karatsuba Multiplier Using Non Linear Carry Select Adder. *Journal of VLSI circuits and systems*, *4*(2), 22-29.

[7] Seyedi, S., & Jafari Navimipour, N. (2022). Designing a multi-layer full-adder using a new three-input majority gate based on quantum computing. *Concurrency and Computation: Practice and Experience*, *34*(4), e6653.

[8] Xu, Xiaofang, Hao Zhang, Jingyu Huang, Nan Zhai, and Yaqi Liu. "Logic gate and optical half-adder designed by photonic crystal based on BPSK signals." *Optik* 259 (2022): 168984.

[9] Anushkannan, N. K., Mangalam, H., Rathish, C. R., & Kumar, A. (2023). Design, simulation, and optimization of optical full-adder based on Mach–Zehnder interference. *Optics Communications*, *528*, 129056.

[10] R. R. Vallabhuni, G. Yamini, T. Vinitha and S. S. Reddy, "Performance analysis: D-Latch modules designed using 18nm FinFET Technology," 2020 International Conference on Smart Electronics and Communication (ICOSEC), 2020, pp. 1169-1174, doi: 10.1109/ICOSEC49089.2020.9215341.

[11] P. A. Gowri Sankar, "A Novel Ternary Half Adder & One Bit MultiplierCircuits based on Emerging sub-32nm FET Technology," 2018 International Conference on Intelligent Computing and Communication for Smart World (I2C2SW), 2018, pp. 198-203, doi: 10.1109/I2C2SW45816.2018.8997120.

[12] D. R. Premachand, U. Eranna and H. P. S. Abdul Lateef, "Design of Area Effective Full Adder Using Gate Diffusion Input Logic," 2018 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), 2018, pp. 1515-1518, doi: 10.1109/ICEECCOT43722.2018.9001388.

[13] D. R. Premachand, U. Eranna and H. P. S. Abdul Lateef, "Design of Area Effective Full

Adder Using Gate Diffusion Input Logic," 2018 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), 2018, pp. 1515-1518, doi: 10.1109/ICEECCOT43722.2018.9001388.

[14] S. Sarkar et al., "Low Power implementation of Multi-Bit Hybrid Adder using Modified GDI Technique," 2018 2nd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), 2018, pp. 1-7, doi: 10.1109/IEMENTECH.2018.8465259.

[15] K. D. Shinde and J. C. Nidagundi, "Design of fast and efficient 1-bit full adder and its performance analysis," 2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), 2014, pp. 1275-1279, doi: 10.1109/ICCICCT.2014.6993157.

[16] S. Nagaraj, G. M. S. Reddy and S. A. Mastani, "Analysis of different Adders using CMOS, CPL and DPL logic," 2017 14th IEEE India Council International Conference (INDICON), 2017, pp. 1-6, doi: 10.1109/INDICON.2017.8487636.

[17] D. S. Rashmi, R. S. Rukhsar, H. R. Shilpa, C. R. Vidyashree, K. D. Shinde and H. V. Nithin, "Modeling of adders using CMOS and GDI logic for multiplier applications: A VLSI based approach," 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016, pp. 1-6, doi: 10.1109/ICCPCT.2016.7530213.

[18] S. Lakshmi, C. Meenu Raj and D. Krishnadas, "Optimization of Hybrid CMOS Designs Using a New Energy Efficient 1 Bit Hybrid Full Adder," 2018 3rd International Conference on Communication and Electronics Systems (ICCES), 2018, pp. 905-908, doi: 10.1109/CESYS.2018.8723899.

[19] S. Malipatil, V. Maheshwari and M. B. Chandra, "Area Optimization of CMOS Full Adder Design Using 3T XOR," 2020 International Conference on Wireless Communications Signal Processing and Networking (WiSPNET), 2020, pp. 192-194, doi: 10.1109/WiSPNET48689.2020.9198627.

[20] G. Nayan, "A Comparative Analysis of 8-bit Novel Adder Architecture Design using Traditional CMOS and m-GDI technique," 2019 International Conference on Communication and Electronics Systems (ICCES), 2019, pp. 128-135, doi: 10.1109/ICCES45898.2019.9002573.

[21] G. Liu, L. Zheng, G. Wang, Y. Shen and Y. Liang, "A Carry Lookahead Adder Based on Hybrid CMOS-Memristor Logic Circuit," in IEEE Access, vol. 7, pp. 43691-43696, 2019, doi: 10.1109/ACCESS.2019.2907976.

[22] S. Vidhyadharan and S. S. Dan, "An Efficient Ultra-Low-Power and Superior Performance Design of Ternary Half Adder Using CNFET and Gate-Overlap TFET Devices," in IEEE Transactions on Nanotechnology, vol. 20, pp. 365-376, 2021, doi: 10.1109/TNANO.2020.3049087.

[23] M. Hasan, U. K. Saha, A. Sorwar, M. A. Z. Dipto, M. S. Hossain and H. U. Zaman, "A Novel Hybrid Full Adder Based on Gate Diffusion Input Technique, Transmission Gate and Static CMOS Logic," 2019 10th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2019, pp. 1-6, doi: 10.1109/ICCCNT45670.2019.8944888.

[24] Mewada, Manan, Mazad Zaveri, and Rajesh Thakker. "Improving the performance of transmission gate and hybrid CMOS Full Adders in chain and tree structure architectures." Integration 69 (2019): 381-392.