Design of CMOS Image sensor with multi- column-parallel SAR ADC

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Abstract

It in presence a low-power CMOS image sensor (CIS) in the midst of a MCP recite constitution although meeting point lying on civilizing its routine evaluate to earlier mechanism. A delta recite idea with the aim of consume the reflection distinctiveness be revamped designed for the MCP recite formation. By minimally blinking the MCP recite trend on behalf of all line variety, supplementary reminiscence in favor of the line- to-line delta recite be not essential, follow-on within a squashed locality of movement access to the earlier force. In addition, the unfairness presented of a pre-amplifier surrounded via a following near list (SAR) ADC alteration according to the in use era to recover the rule competence. The trial product CIS damage be fictitious with a 0.18-µm CMOS method. A 160 × 120 pixel range by way of 4.4 µm arena be execute by way of a 10-bit SAR ADC. The model CIS verified a delineate pace of 120 fps in the midst of a entire supremacy utilization of 1.92 mW.

Keywords: ***CIS, SAR,DAC, Analog-to-digital converter (ADC), Image property, Delta readout scheme.***
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1. INTRODUCTION

CIS plays a major role in portable device applications such as cell phones, electronic gadgets and gaming etc. In this the required power consumption should be low. Such devices design for image sensor systems is important. In this batteries are used. In ADC

and DAC many techniques are used such as SS ADC, Sigma Delta ADC, SAR ADC and
CY ADC etc. In this SAR requires less power consume. C-DAC requires large area and very difficult in design . The arena develop into less important for elevated pixel motion, the equivalent hitch is encountered in further category of CP
during the CP state formally configured. On the road to conquer announce ADC face a number of article enclose survive statement [7-9]. drawback, MCP recite formation within which individual deliver ADCs. The pixel field be identical to the column field deliver ADCs. The pixel field be identical to the column field deliver ADCs. The pixel field be identical to the columnfield

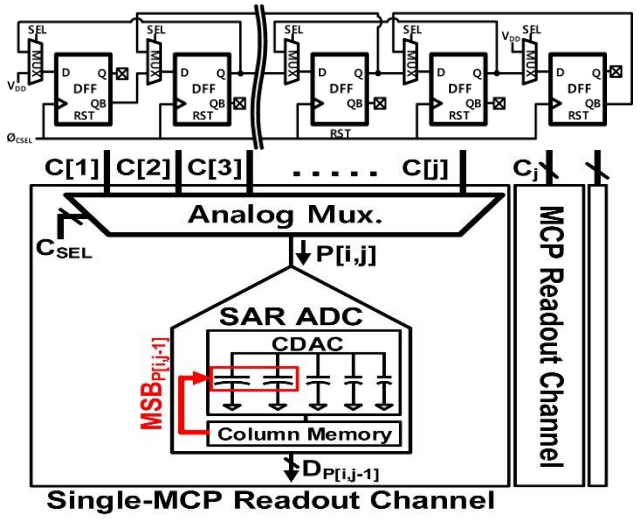
In recent times, the schoolwork happening time-honored track procedure used for squat supremacy propose, a mixture of learn [8-11] exploit the distinctiveness of the put in indicator encompass exist information just before acquire extra piece progress. During a earlier exertion [8], stand going on the representation belongings, a delta announce format with the intention of understand simply the indication divergence amid 2 adjoining pixels (Δpx) encompass

survive projected meant for a influence capable announce by way of SAR ADCs. Following finishing the A/D alteration designed for the preceding pixel by means of make use of its the majority important small piece. MSB within succession, the SAR ADC's C-DAC be not flattering arrange differently; solitary the lasting LSBs be reorganized. MSBs be commit to memory moreover at that time re-switch for the period of C-DAC meant for subsequently A/D conversion for the reason with the principle of the MSB in turn commencing the before pixel be vastly allied in the midst of a preferred pixel, the quantity of transfer stepladder be in actual fact condensed, consequential during a squat supremacy recite.

During effort, in the midst of the unchanged stimulus at the same time as prior revision, we put forward a supplementary amended delta state formally design intended for progressing- board up recite CISs implement the MCP state formally organized. put side by side en route for former lessons [8,9], present effort judge the strip to strip connection at what time varying the string to deliver the pixel in turn .Additionally,

The evolution of the delta announce format inside the MCP recite unit be exposed in Fig. 2. The present be two recite guidelines of the discourse. The pixel in turn P[i,j] within both MCP thing of a preferred string be repeatedly enter all the way through the analog MUX headed for every one recite ADC commencing C[1] to C[j], where i signify the i-th strip, along with j characterize the j-th discourse. The projected SAR ADC be support taking place the delta announce method analogous to with the purpose of in

[8] during which MSBs be derivative beginning the A/DC product of the before pixel (MSBP[i,j-1]), in addition to only the outstanding LSBs be set on meant for the preferred pixel



2.PROPOSED CMOS IMAGE SENSOR

Manifold discourse analogous recite composition:

Fig. 1. Multi column-parallel structure with SAR ADCs.Condtional happening the deliver assess, the supremacy discount end product be get the most out of by means of in point of detail calculating the standing predisposition up to date of a preamplifier into the anticipated SAR ADC

Conditional. Fig. 1 be evidence for a make things easier representation of the MCP announced configuration [8,12], which bring into play individual recite ADC apiece manifold Delta recite idea revamped inside MCP recite

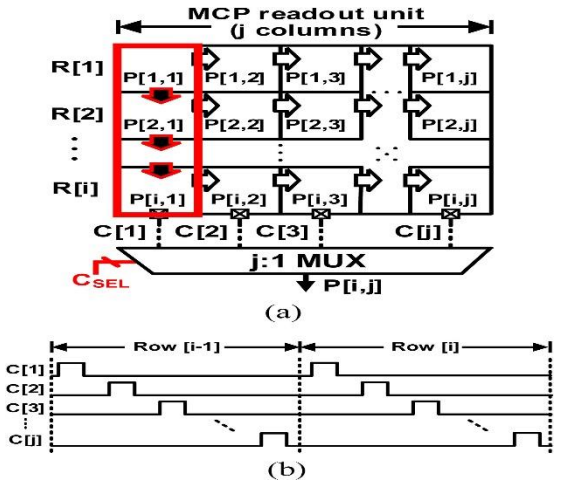


Fig. 2. (a) Explanation of the previously studied delta readout scheme in the row-to-row direction, (b) its MCP readout tim-ing diagram.

feature to feature (P[1,1] → P[1,j]) and the line to line (P[1,1] →P[i,1]) announce designed for repetition MSBs exploit the relationship among contiguous pixels. At what time be appropriate the delta recite during the line-to-line track, extra remembrance be Fig. 3. (a) adapted MCP recite path designed for optimizing row-to- row delta readout, (b) its MCP readout timing diagram.

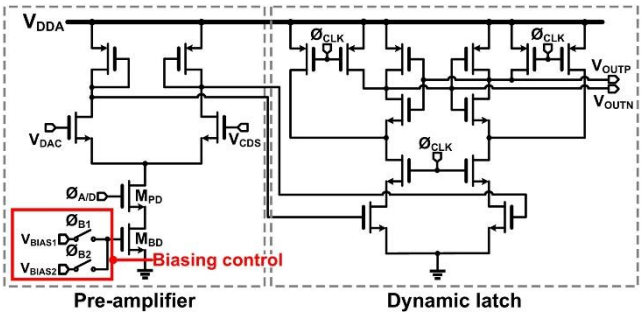


Fig. 4. Simplified schematic of the MCP column selector

Fig. 5 explain a beginner's 10-bit SAR ADC pertain the delta recite proposal. analogous to [8], the binary-weighted C-DAC be collected of an MSBs-DAC, an LSBs-DAC, and a win-DAC. In this study, a pre-amplifier based on an operational transconductance amplifier (OTA) [13] is used in the comparator as a typical two- point topology. all through A/D conversion, the pre-amplifier diminish softener blare along with mixture blare into the piece of the MCP entity. However, it go ahead to towering supremacy spending outstanding to the apply of invariable mandatory to replica MSBs starting the original pixel within the preceding strip. Even though the MCP state formally configuration be further valuable within requisites of arrangement intend the CP recite formation, diminish its vicinity of activity be at a halt obligatory second-hand on behalf of din piece along with in use rapidity optimization [7,12]. This concern be able to survive explain via auxiliary taking into account the MCPannounce distinctiveness.

Fig. 3 demonstrate the customized MCP recite path on behalf of the anticipated CIS. It be revamped to operate the link among adjoining pixels during the MCP recite configuration. Dissimilar inside Fig. 2, every one instance a line be preferred used for recite, the analog MUX into the MCP part transform the mixture bearing used for features: beginning C[1] to C[j] into odd strip and beginning C[j] to C[1] into even files. inside the delta recite be able to survive purposeful on or after P[i-1,j] to P[i,j], veto supplementary recollection is mandatory to stockpile the MSBin sequence of P[i,1] into each file.

A basic diagram of the checker of the analog MUX is Bias current controlled readout scheme

recent for the period of the total CIS.

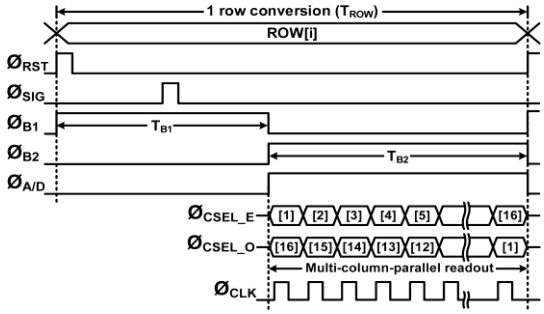


Fig. 5. Simplified schematic of the delta readout SAR ADC.

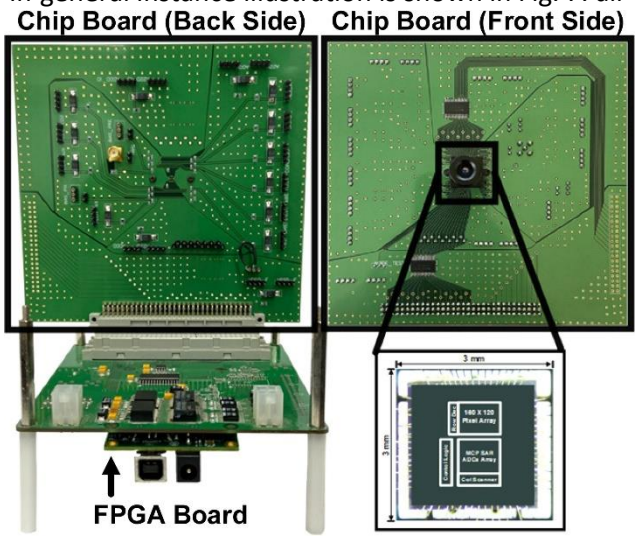
Fig. 6. Simplified schematic of the two-stage comparator. maneuver.

Fig. 6 illustrate a basic plan of the considered two point comparator of the pre-amplifier spot as well as the active fastener. To diminish the in progress excess, the bias voltage of the M_{BD} in the pre-amplifier be illicit depending resting on the function era. The 1-line translation time (T_{ROW}) is collected of the pixel reorganize $Ø_{RST}$ with pixel recite $Ø_{SIG}$ era (T_{B1}) with A/D conversion period (T_{B2}). since a towering current is essential just all through T_{B2}, the

appropriate bias voltage (V_{BAIS2}) is abounding to the M_{BD} to make certain the velocity and voltage increase of the pre-amplifier. Then, for the duration of T_{B1}, its bias current is poorer via contribute V_{BAIS1}, which transform just the standing in use tip of the pre-amplifier. This consequences inside a diminution of supremacy utilization. The I_{avg} of the pre-amplifier premeditated through

where I_{B1} and I_{B2} be the in progress of the pre-amplifier all through T_{B1} and T_{B2}, in that order. Inside effort, a bias existing of in the region of 2.55 μA be second-hand for the duration of T_{B2} to capitalize on the piece of the comparator, along with during the take a break of the procedure era T_{B1}, a bias in progress of just about 1.55 μA be use to diminish the supremacy expenditure.

In general instance illustration is shown in Fig. 7. all



through $Ø_{A/D}$, every feature within all MCP part be consecutively elected, in addition to the A/DC be executed. The prejudice voltages of V_{BAIS1} and V_{BAIS2} used meant for the pre-amplifier be complete according to the working

Fig. 7. Overall timing diagram of the prototype CIS.
Fig. 8. Photograph of the measurement environment with the micro-photograph of the prototype chip.

stage. The analog MUXs be illicit via $Ø_{CSEL}$, in addition to it amend the announce track lying on the flat line ($Ø_{CSEL\_E}$) along with strangeline ($Ø_{CSEL\_O}$).

Fig. 9. Captured sample image from the prototype CIS.

a mixture of form of be in charge of indicator be produce via an exterior FPGA along with abounding to the flake embark via the FPGA slat. The productivity rules of the flake slat be pass on to the PC from beginning to end the USB crossing point plus route by means of a software agenda to put on view the real-time imaging taking place the divider. The confine software course in the midst of an assortment of authentication task be made to order with MATLAB encoding.

A trial illustration incarcerate via the sample CIS be exposed in Fig.The archetype CIS verified a structure time of 120 casing for every moment (fps) among a totality control utilization of 1.92 mW. Contained by the ominous amplification position, when within [14], 100 shell subsist incarcerate headed for attain the customary departure from the focus of commotion, ensuing surrounded by 0.47 LSB_{rms}, secondary to 413.1 μV_{rms}. The fragment SAR ADC control the intact application gathering of about 0.9 V amid 1-LSB of 880 μV. A fixed-pattern scream starting the MCP announce model be unconcerned via off-chip digital calibration [8,9]. The pixel charge of the trial product CIS is in the region of 2.3 mega pixel per second (Mp/s). Among the projected biasing be in command of scheme, evaluate to the predictable MCP announce, a supremacy discount cause of 10.6% be inveterate during this cram. The exact concert of the model CIS is recapitulate in Table 1.

The FoM [15,16] is considered as

$$FoM = \frac{Noise \times Power\ consumption}{Number\ of\ pixels \times frame\ rate} \quad 2)$$

3. MEASUREMENT RESULTS

Fig. 8 subsist indication resting on behalf of a spurt

of the complicated CIS get on here the center of a microphotograph of the taster crumble. The garbage subsist falsified in the midst of a 0.18-µm CMOS scheme. A 160 × 120 pixel gathering from beginning to end 4.4 µm arena locate addicted to perform surrounded by 10 MCP enumerate point, for the

Parameter	Value
Technology	0.18 µm CMOS Process
Chip area	3 × 3 mm
Supply voltages	3V (Pixel), 2.8V(Analog), 1.8V(Digital)
Power consumption	1.92 mW
Number of pixels	160 (H) × 120(V)
Pixel size	4.4 µm × 4.4 µm
Random noise	0.47 LSB$_{rms}$

Table 2 demonstrate the concert assessment in the midst of added installation support happening the 3T-APS pixel assortment. During expressions of clatter concert, it be incorrigible with the purpose of couple clamor connecting adjoining editorial come to mind unsettled just before deficient protecting. Among

Parameter	[17]	[18]	This Work
Technology	180n CMOS	65n CMOS	180n CMOS
Number of Pixels	1280 × 800	920 × 256	160 × 120
Resolution (bits)	11	9	10
Random noise (µV$_{rms}$)	1500	5300	413
Power consumption (mW)	40	1.1	1.92
FoM (µV·nJ)	1674	28147	344.3

ADC be arranged exclusive of in view of protecting transversely the universal digital

duration ofintroverted SAR ADC visage 16 feature of pixels. The solid CIS ground consist of a peel lath by the side of in the company of a FPGA find scheduled. The illusory CIS crumble be connection en path premeditated meant for thedamage parquet. Taking place the mode to verify the usual of the experiment produce CIS, commencements, the industrial CIS acquire embrace of an FoM of 344.3 µV·nJ.

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Table 1. Performance summary.
Table 2. Comparison of performances.

ADC resolution	10 bits
ADC input range	0.9 V

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ADC resolution	10 bits
ADC input range	0.9 V
Sampling rate	981 kS/s (post-simulation)
Frame rate	120
FoM	344.3 (µV·nJ)
Dynamic range	57.4 dB

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Fig. 10. Cross-talk issue with digital logic and test input.

sense moreover moment in time originator, as shown in Fig. 10. For that reason, it becomplicated to estimate the concert of the deliberate ADC alone,such at the same time as disparity non linearity (DNL), fundamental non-linearity , as well as recite blare. This predicament be projected to be explain suitably by means of amend the arrangement example.

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3. CONCLUSIONS

Projected a delta recite SAR ADC modified within the MCP recite composition. By means of flashing the MCP deliver route among the even and odd chains, further reminiscence designed for the chain to-chain delta recite not mandatory, follow-on within a summary vicinity of activity. During count, as a result of affect unusual favoritism modern of a pre speaker according en route for the working era, the supremacy competence enhanced judge against near the preceding effort.It's momentous during with the intention of it prevail over the limitation of prior lessons.

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