T-TYPE CONVERTR HARMONIC REDUCTION USING FILTER FOR GRID APPLICATIONS

G.Muli Naidu [1],T.Phanimala[2], T.Srilatha[3]

[1]Assistant Professor, Department of EEE, Vignan's institute ofengineering for women affiliated to JNTUK, Kapujaggarajupeta, Duvvada, Visakhapatnam, Andhrapradesh,India.

[1]Assistant Professor, Department of ECE, Aditya College of Engineering affiliated to JNTUK,Surampalem,Andhrapradesh,India.

[1]Assistant Professor, Department of ECE, vignan institute ofengineering for womenaffiliated toJNTUK, India.

Abstract:

To ensure good power quality, multilevel inverters (MLIs) have emerged as the preferred option for low- and medium-power dc to ac energy conversion applications. In comparison to the traditional two-level inverter, the MLIs have a number of advantages, less electromagnetic interference, including a lower dv/dt, and the ability to handle greater voltage levels with equipment with a lower voltage rating.Due to these qualities, they have become more popular in a range of industrial applications, including, but not limited to, locomotives, mixers, marine propulsion, reactive power compensation, and renewable energy power conversion. The need to produce a significant number of voltage levels while maintaining the highest feasible level of circuit reliability served as the driving force behind this research project. As a result, a new topology, the three phase T-Type converter, is built in this study by utilizing the fundamental MLI configurations.

Key words: MLI, T-Type converter, dv/dt, THD, NPC, LC filter

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Introduction:

Recently, there has been a lot of interest in energy conversion in the low voltage region. Automotive inverters, PFC rectifiers, and photovoltaic grid inverters are just a few examples of applications. Systems using inverters must be very efficient while being inexpensive. must have passive components that are small and affordable. The switching frequency is frequently raised to a medium level range of 12–25 kHz, which causes higher switching losses and worse efficiency. System effectiveness Acoustic noise might also be a problem. Avoid attempting to decrease acoustic noise. essential in aeroplane applications and high-speed drives. It's typical to use high control and output frequencies up to 1 kHz. A requirement for bandwidth exists. Here, the exchanging is completed.Multilevel topologies exhibit a significant degree of complexity, according to earlier study. The relationship between the converter's efficiency and switching frequency is linear [1, 2]. This study demonstrates the 3-level T-type converter's (3LT2C) aggressiveness in low-voltage situations. The T-type topology has two fewer diodes per bridge leg and an active bidirectional switch at the dc-link voltage midpoint than the three-level NPC topology. Compared to active neutral point clamped converters [9]–[11] or split-inductor converters [12], [13], it has a simpler three-level architecture.

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The 3LT2C combines the advantages of three-level converters, such as lower switching losses and improved output voltage quality, with the advantages of two-level converters, such as low conduction losses, a compact part count, and an easy-to-understand operational concept. A three- level voltage source converter (VSC) built with 1200-V IGBTs is compared to a VSC built with 1200-V IGBTs if a two-level voltage source converter is employed. If the neutral point clamped (NPC) converter is built with 600-V devices, the three-level converter's efficiency can be increased. Because of the low switching losses and high efficiency of the 3LT2C, the lowered conduction losses are reduced. This word is often used in industry, particularly at switching frequencies between 8 and 24 kHz. Without, this is accomplished.The 3LT2C is considered to be a competitive alternative to two-level converters in applications where greater efficiency is required. Increasing switching frequency and efficiency is a key objective.Adding to the conventional two-level VSC architecture is the dc-linkmidpoint. The single-bridge leg of the T- type VSC resembles the rotated letter "T," therefore the name of the topology.

II. METHODOLOGY

a) T-Type topology

The fundamental architecture of the 3LT2C is shown in Figure 1. The conventional two-level VSC design is extended by the addition of an active, bidirectional switch to the dc-link midway. In low-voltage applications (where Vdc = 650 V, for example), the full dc link voltage must be blocked, hence the high side and low side switches (T1/D1 and T4/D4) are typically implemented using 1200-V IGBTs/diodes. On the other hand, the bidirectional switch to the dc- link midpoint only needs to block half of the dc link voltage. Lower-voltage devices can be used to implement it; for instance, in the current scenario, two 600-V IGBTs with antiparallel diodes are used.Due to the lower blocking voltage, the middle switch has acceptable conduction losses and very low switching losses despite being coupled in series with two other devices.

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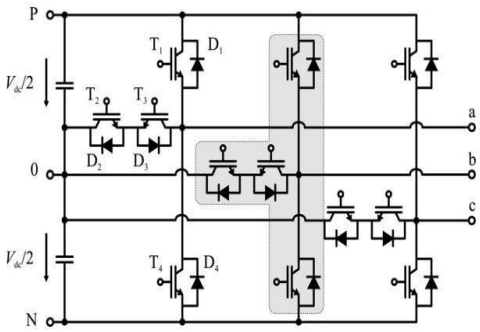

Fig 1:.The three-level T-type topology is depicted in this diagram

b) Switching configuration

To create a bidirectional switch, the two 600-V IGBTs can be arranged in either a common emitter configuration or a common collector configuration. The common emitter setup [cf., Fig. 2(a)] would call for three additional gate drive supplies, or one more isolated gate drive supply voltage, compared to the two-level VSC design.

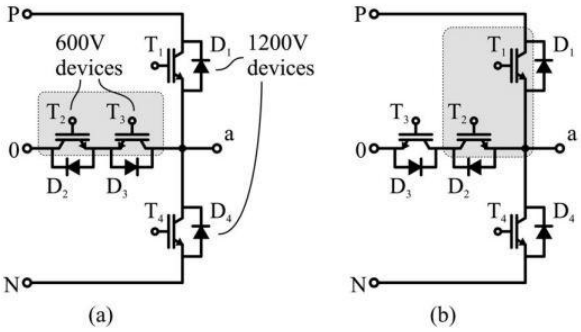

Fig2:TwoIGBTsinacommonemitterorcommoncollectorarrangementcanbeusedtobuildabidirectionalswitchto themiddle

This number can be reduced even more if common collector architecture is used. With T1's isolated gate drive voltage acting as its source of power, T2 now shares an emitter with it on the high side. The emitter of the second 600-V IGBT is connected to the middle voltage level. The three IGBTs T3, a, b, and c share a common emitter when the three-phase architecture is taken into account, necessitating just a single isolated gate drive supply. The entire T-type topology can be obtained with just one more isolated gate drive supply in comparison to the two-level layout.

c) Switching Sequence:

The given Table 1.shows the operating states or switching states and generated voltage levels. There are three controls objectives for three level T-Type rectifier.There objectives are regulation of DC voltage (Vdc) , control of line currents such that they are in phase with the corresponding grid voltages andcompensation of imbalance between DC capacitor voltages. Consider k=(a,b,c).

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Table-1. Switching sequence of a T-type converter

Operating State	S1k	S2k	S3k	S4k	Vko
P	ON	ON	OFF	OFF	Vdc/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

III. SIMULATION

a) SystemSimulation model

The obtained analytical model for the neutral point current in the T-type three level PWM converter was validated by simulation and experimental tests. Phase locked loop (PLL) was used with three phase grid voltages to measure the grid's phase angle and frequency. The parameters of the complete system are summarized in Table 2.

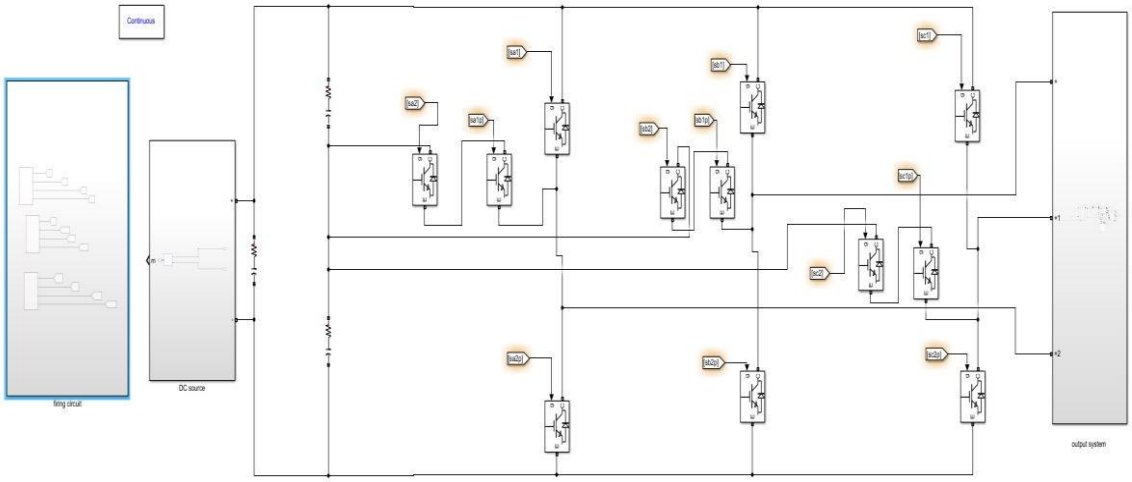

Fig.3. T-Type converter Matlab simulation model

In the above system model it consisting of T-Type converter which converts DC source given from the battery to AC output, based on the firing angle given from the firing circuit. And all the system parameters are summarized in the table -1 given below

Table-2.Summarized tablefor a complete system parameters.

ELEMENTS	PARAMETERS RATING
battery	Nominal voltage=650*2.56 Rated capacity=1.5Ah Response time=30 Sec
Series RC circuit	R= 10 Ohms C=1mF

IGBT	Internal resistance=1m Ohm snubber resistance=100k Ohm snubber capacitance=infinity
LC Filter	L=4Mh RMS Voltage= 380V Reactive power= 8Kvar

Low pass filter	Cut off frequency= 100Hz Damping factor=0.707
Total harmonic distortion	Frequency=50Hz Sample time=10^-5 sec
modulation index	1 (Vr/Vc)
RC	0.1000
Start time	6*10^-5 sec
Vdc	(0-1000) V
C	0.4m F

b) Gate driving circuit

Fig.4 is simulation model for the firing circuit which works based on the pulse width modulation technique. Based on the number of pulses and pulse width, the output average voltage will depends.Here in witch it contains reference signal and carrier signal by which the width of the pulse can be determined.

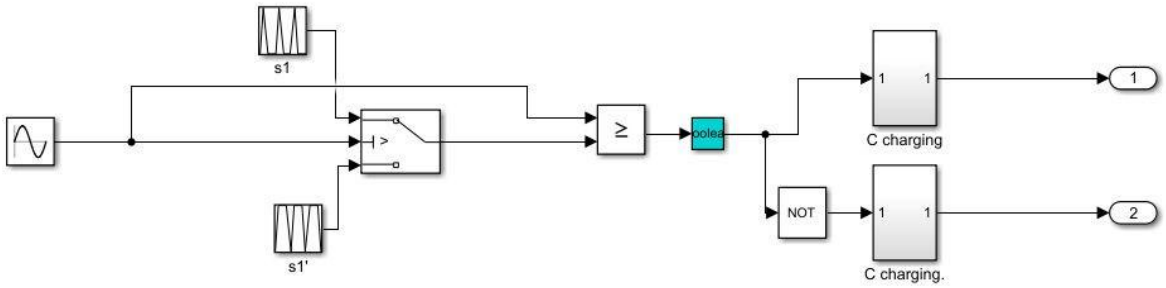

Fig .4.simulation gate driving circuit for T-Type converter

IV. SIMULATION RESULTS

Fig 5.shows inverter line voltage. P, O, and N are the three levels. This waveform corresponds to theinformation in table 2. The volatility of the dc-link capacitor voltage can be seen in this diagram. This is duetothe dc buscapacitorvoltagebeingunbalanced.

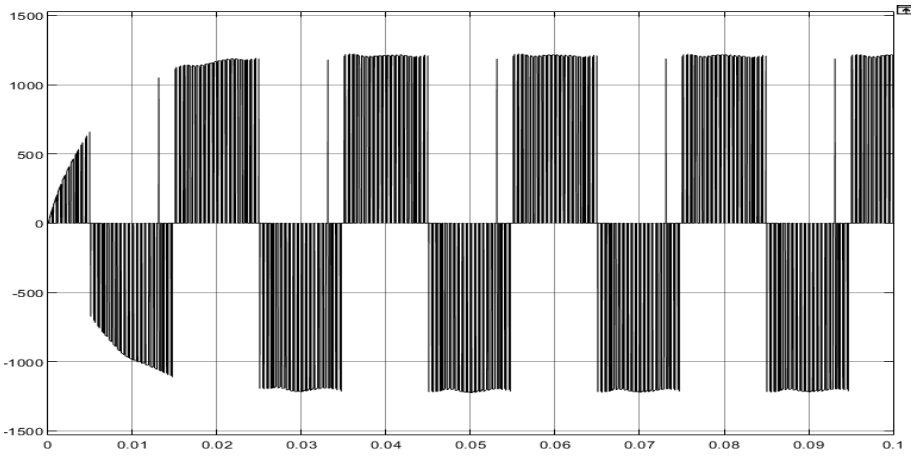

Fig. 5.output line to line voltage across T-type converter

Fig 5 shows the inverter line voltage. It is divided into five levels. This voltage waveform has a substantiallylower harmonic than a traditional two-level inverter with the same switching frequency. When the dc linkvoltageis extremelyhighorthe gridvoltage isextremelylow, thewaveformmayonlyhavethreelevels.

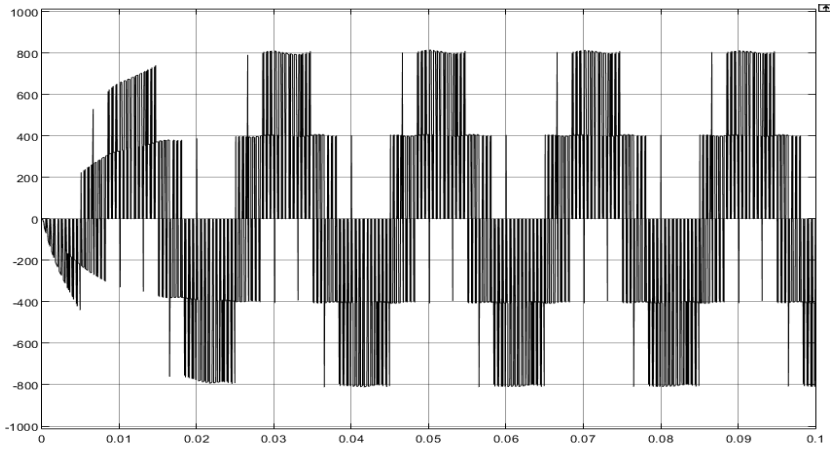

Fig .6.output across the load from T-type converter without filter circuit

Figure 6.shows the total harmonic distortion without using any filter circuit and THD value is 53.12%.and the THD value can be reduced using LC filter at the load end side which can reduce the THD value from 53.12% to 0.9%.

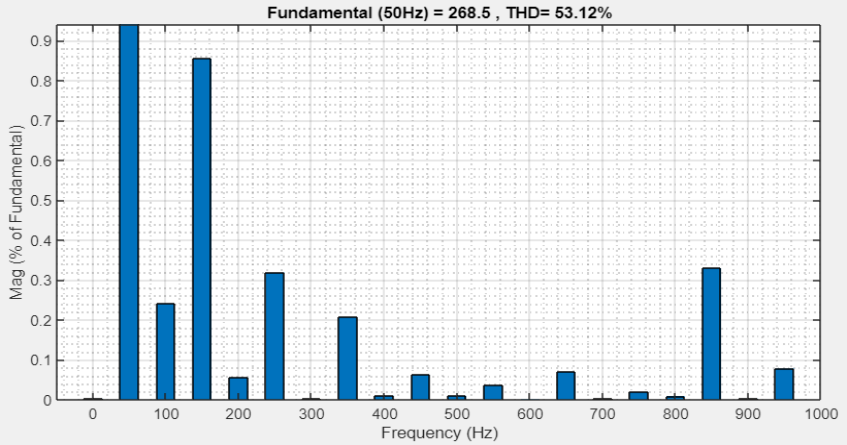

Fig 6. THD without filter circuit

Fig7showsfilteredlinevoltages.Itisdisplayedforeachofthethreevoltages.Thesewaves werecreatedwiththeuse of afilter.Fig 8.Shows the Reduced total harmonic distortion with LC filter.

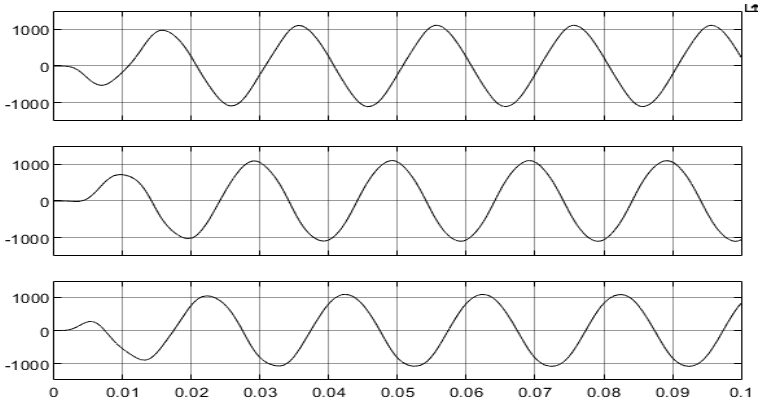

Fig.7. output from T-type converter with filter circuit

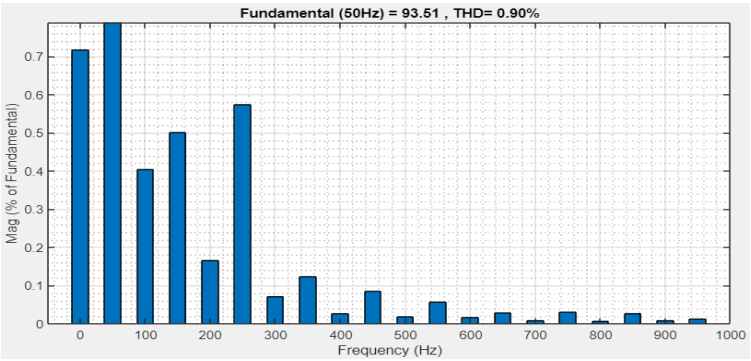

Fig.8 THD with filter circuit

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V. Conclusion

In this work, the three level three phase converter was introduced for high-efficiency low-voltage applications. It is a two-level VSC solution for applications requiring medium switching frequencies, and it performs especially well between 4 and 30 kHz. The main advantage is that switching losses are reduced as compared to a two-level arrangement thanks to a halved commutation voltage. The conduction losses are not much different.A bidirectional switch at the dc-midpoint link was investigated using two anti-serial 600-V IGBTs in common-emitter or common-collector configurations. The advantages of the additional isolated gate drive supply for the common-collector option were also shown. There was a straightforward, current-direction-independent commutation method given. And in this paper the three level three phase converter was designed with A high efficient LC filter circuit which can reduce the harmonic distortion in the T-type converter output voltage. THD value can be reducefro 53.12% to 0.9% with the help of LC filter circuit.

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